Rethinking the Role of Power and Return Planes

There may be a better use for PCB planes than to just distribute power, namely to provide shielding.

by Glen Dash, Ampyx LLC

To begin, we will test the circuit shown in Figure 1 for its EMI characteristics. A clock driver, running at 25 MHz and using HC technology, drives an HC load. Techniques commonly thought of as good EMC practice are used throughout. A wafer-type low inductance capacitor is placed beneath each IC. The run connecting the clock to its load is straight and placed immediately adjacent to the return plane. A damping resistor is in use. Telescoping antenna elements are connected to the return plane and extend out 19 inches from either edge of the board simulating the use of I/O cables. The telescoping elements are set to produce a system resonance at 125 MHz, the 5th harmonic of the clock.

We also covered both the top and the bottom of our circuit with copper foil creating what are, in effect, shields on the top and bottom. Everything is covered, the batteries, the ICs and the connections between the clock driver and its load. The device is shown in Figure 2 (page 34). Solder was used to ensure a good electrical connection where seams of the copper tape came together, which accounts for the rough appearance.

Emission results are shown in Figure 4 (page 34) and are unimpressive.

Why should this circuit radiate so much energy? Part of the reason is that a *complete* shield is not in use. The top shield is still separated from the bottom shield, the top shield being connected to V+ and the bottom shield to V-. There is a gap between V+ and V- represented by the dielectric between the PC board's two planes and it is that gap that makes all the difference.

The source of the radiation can be traced to a phenomenon we have noted elsewhere. When a MOS driver switches, there is a moment during the transition when both the

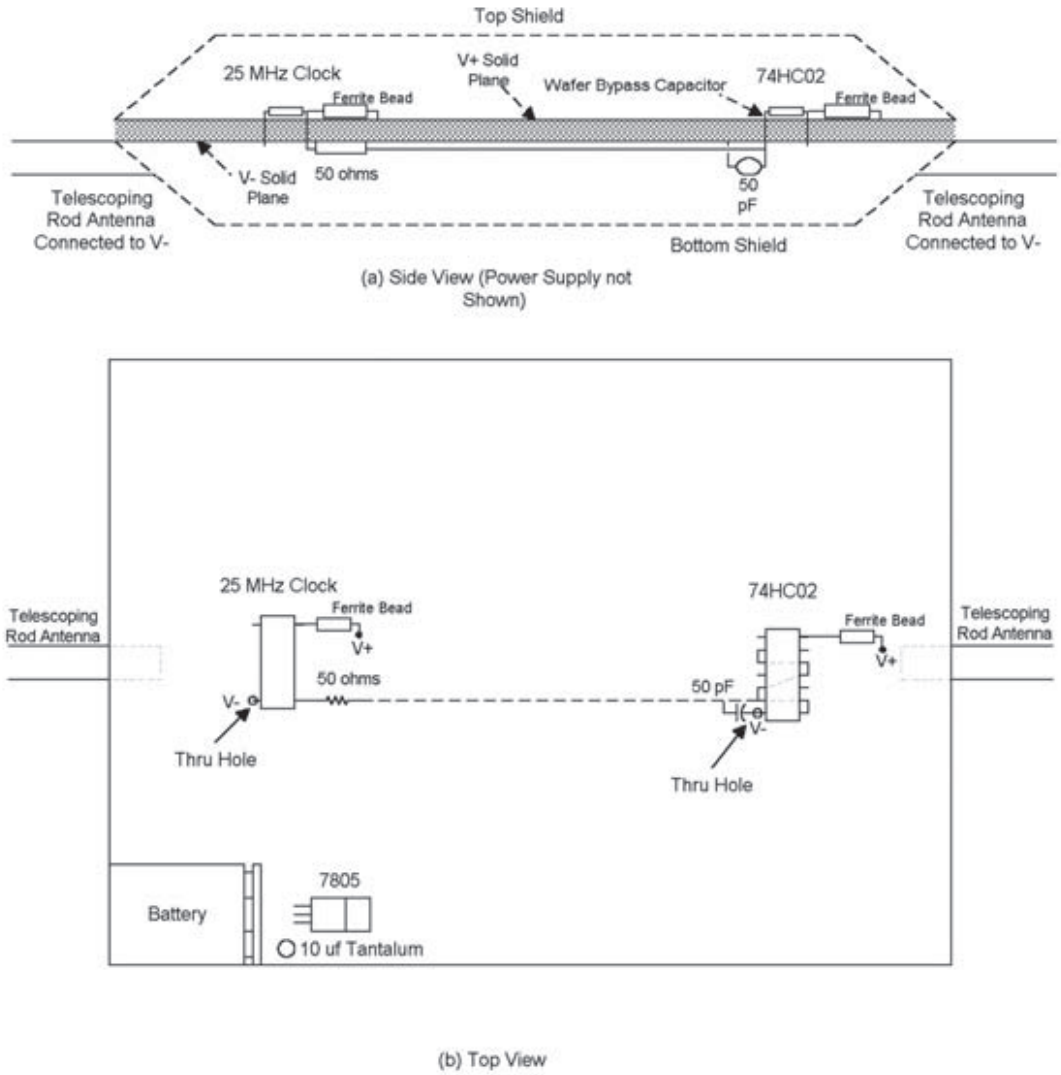


Figure 1: The device we first tested had shields over the top and bottom of the PCB, the top shield connected to V+ and the bottom to V-. The shields were formed with copper tape soldered at the seams.

P and N channel devices are both on. A brief burst of noise known as Idd Delta (or Idd Noise) is produced. This impulse is on the order of hundreds of picoseconds to a few nanoseconds in length and one to ten milliamps in amplitude per gate for most MOS based technologies. This impulse is impressed onto the power planes which can modeled as a kind of parallel plate transmission line. The impedance of a parallel plate transmission line is well known.

It is:

$$Z_0 \cong \left(\frac{d}{w}\right)\frac{377}{\sqrt{\varepsilon_r}} = \left(\frac{d}{w}\right)\sqrt{\frac{\mu_0}{\varepsilon_r \varepsilon_0}}$$

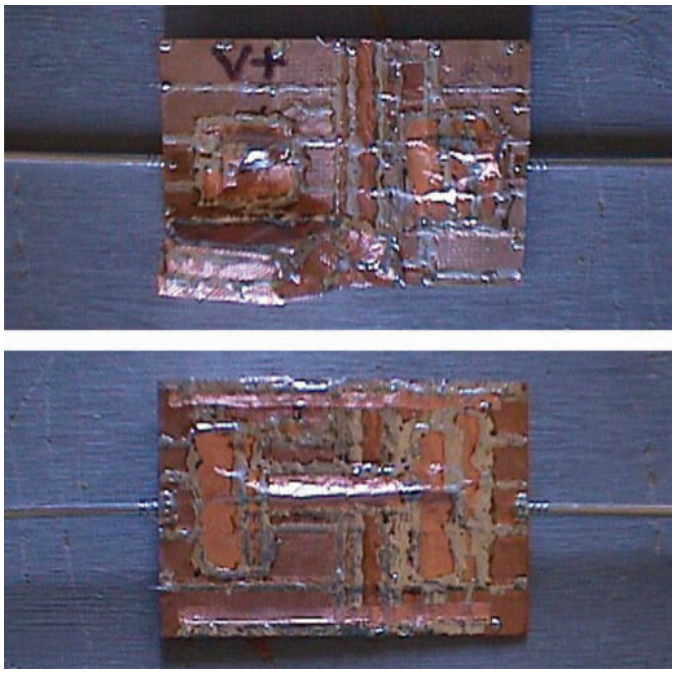


Figure 2: The top side of our experimental circuit carries V+ and the bottom, V-. Components and wires, top and bottom, are covered with foil.

Figure 3: The test setup. Note the telescoping elements used to simulate I/O cables.

Where:

d = Distance between the planes

w = Width of the planes

ε_r = Relative permittivity

ε_0 = Dielectric constant in free space= 8.85 x 10^{-12}

μ_0 = free space permeability = 4π x 10^{-7}

The impedance of a transmission line is also a function of its capacitance and inductance per unit length and is equal to:

$$Z = \sqrt{\frac{L}{C}}$$

Where:

L = Inductance in Henries per unit length

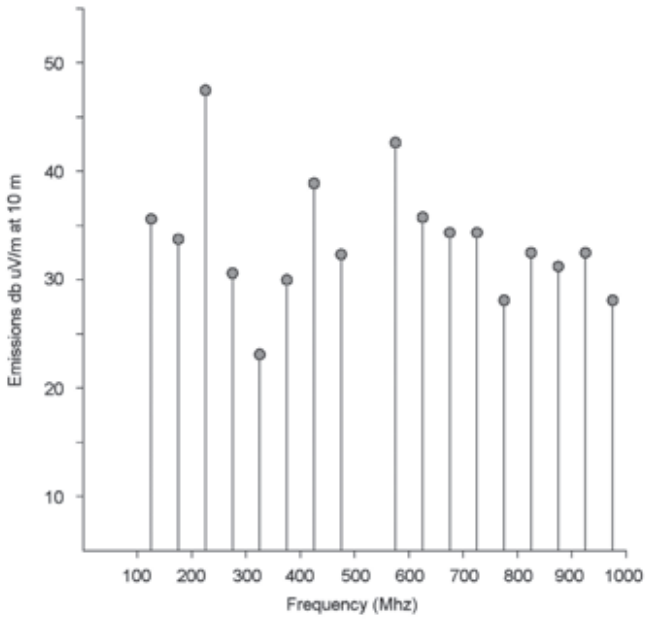
C = Capacitance in Farads per unit length

As for the capacitance per meter of length, that too is well known. Ignoring fringing fields it is:

$$C = \frac{w}{d}\varepsilon_r \varepsilon_0$$

These three equations allows us to derive the approximate inductance per unit length of a parallel plate transmission line:

$$L \cong Z^2 C = \frac{\mu_0 d^2 w}{\varepsilon_r \varepsilon_0 w^2 d}\varepsilon_r \varepsilon_0 = \mu_0\left(\frac{d}{w}\right)$$



Test 1: Top and Bottom Shielded, but Shields not Connected
(See Figures 1 & 2)

Only odd harmonics of the clock were examined.

Figure 4

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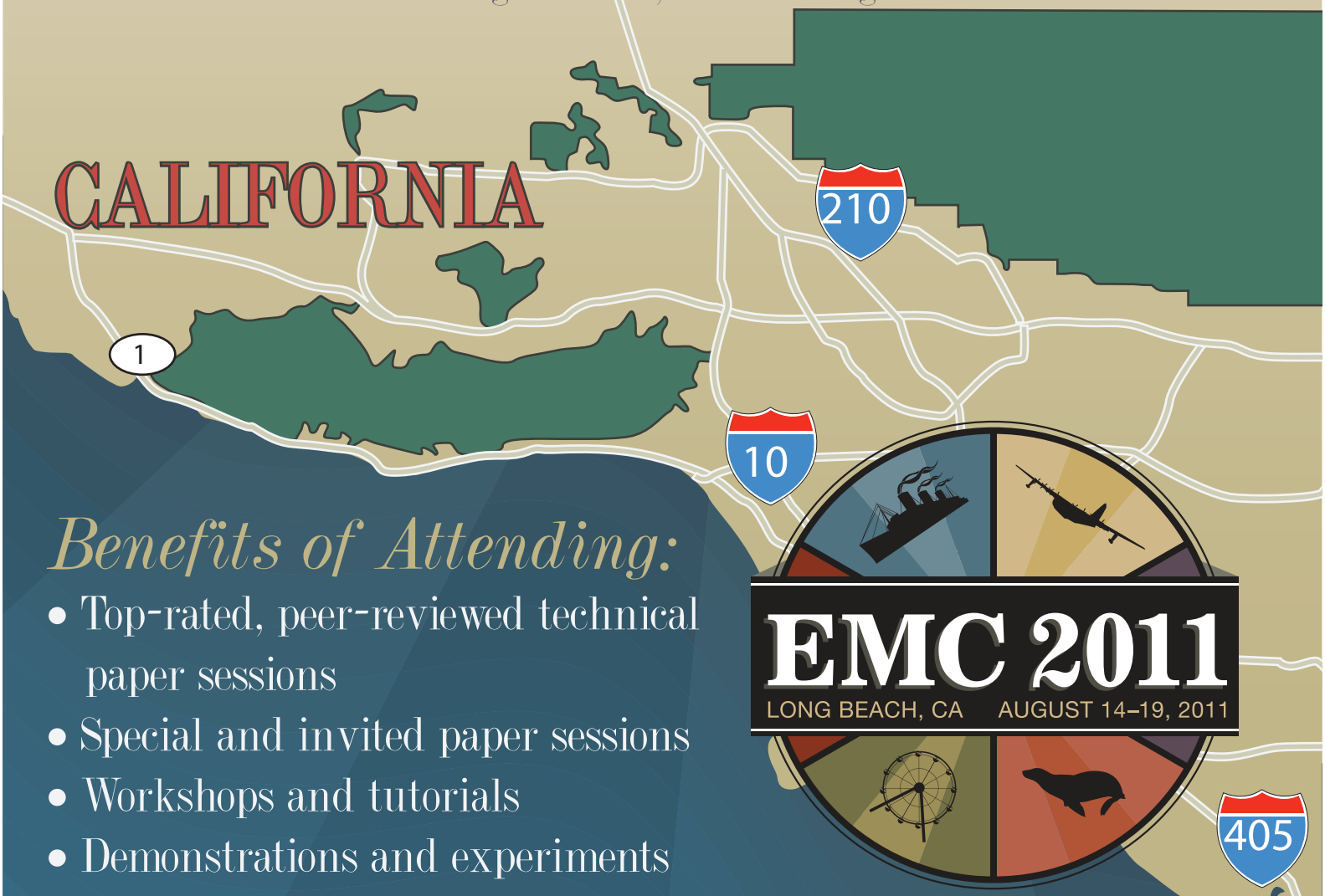

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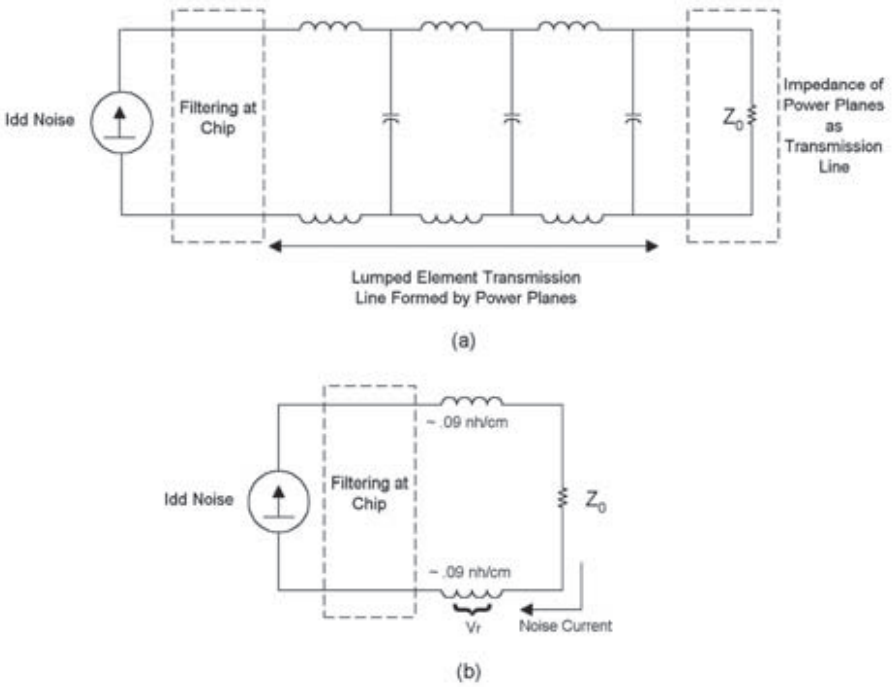

Figure 5: Transmission line characteristics of the power and return planes are modeled here. The model can be simplified as shown in (b).

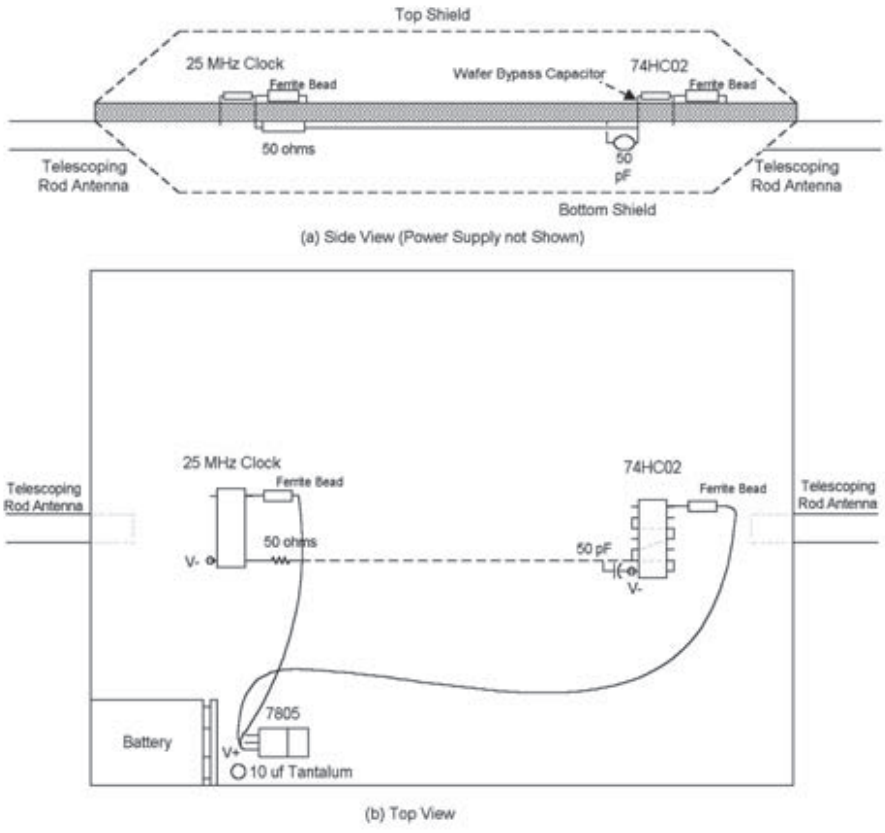

Figure 6: Going somewhat against convention, we sought to lower emissions by hard wiring the ICs to the supply using ordinary wires, isolating the top shield from V+ and then connecting both shields together. Emissions dropped significantly.

It is this inductance that gives rise to our problems, specifically the inductance of the return plane. Since the transmission line is symmetrical, we can assign half the total inductance to the return:

$$L_{\text{return plane}} = \frac{\mu_0}{2}\left(\frac{d}{w}\right)$$

For our circuit, d=1.6mm and w=11.5cm, resulting in a return inductance of approximately .09 nh/cm.

We can use circuit models to describe the phenomenon. In Figure 5a a current source, which we model as impulsive with fundamental frequency of 25 MHz and of a peak amplitude of 1-10 milliamps, drives a nearby filter consisting of a bypass capacitor and an associated ferrite bead. That filter, in turn, is connected to the elemental inductances and capacitances which comprise the transmission line formed by the power planes.

The model helps explain why our shields do not work. Currents passing down the transmission line formed by the power planes result in a voltage drop *across* the return plane. The resulting voltage drop, V_r causes the attached telescopic antennas to radiate like a dipole.

Real world circuits are, of course, more complicated. They act like a transmission lines terminated here and there with bypass capacitors and, at their edges, not at all. That makes emissions difficult to predict. However we can say that the emissions are a function of at least three things: (1) the impedance of the return plane, (2) resonances caused by the combination of various inductances and capacitances, and (3) transmission line effects from the power planes acting as poorly terminated transmission lines.

Some authors have recommended controlling emissions by flattening the impedance presented by power planes. [1] Here we propose a different approach, the use of planes to provide shielding.

At first blush, Figure 6 does not look very much different than Figure 1, but there is a crucial difference. Here the top and bottom shields are connected together and the top shield isolated from the supply. We have routed separate wires from our power supply to the ICs to provide power. This time when emissions are measured, the fall is dramatic (Figure 7). Only one emission is found at all greater than 5 uV/m at 10m, it being at 125 MHz and about 20 dB down from the device of Figure 1.

The reason for the dramatic fall is quite simple, we now have a Faraday cage and it is working the way it should. Figure 7 is simply confirmation of what we already know, that if you put a complete shield around a circuit, it does not radiate very much.

Unfortunately, complete shielding is often not a practical option. In order to evaluate a more practical solution, we removed the shielding over the integrated circuits as shown in Figure 8 (page 38). While radiation did increase, the reduction in emissions was still dramatic (Figure 7).

We also experimented with a serrated connection between the top and bottom shields as shown in Figure 9 (page 38). It had no significant effect on emissions.

We are not contending that a well designed, low impedance power source is not important -- it is. Providing a low impedance, low Q power source is vital to preserving noise margin.

However, it may not be the key to reducing emissions.

In Figure 10 (page 38) we show some PCB stack ups where the outer layers are used for a shield. Figure 10(a), for example, shows a six-layer stack up. The top layer is used to support components.

The second and sixth layers comprise an internal shield. They carry no traces though they will be studded with holes to allow vias. No gaps or openings should be permitted in this shield layer, just holes. The inner layers contain power and circuit layers. These inner layers do not extend to the edge of the board. Instead, a small portion (a centimeter or so) is reserved for a shield ring. Vias connect layer 2 to layer 6.

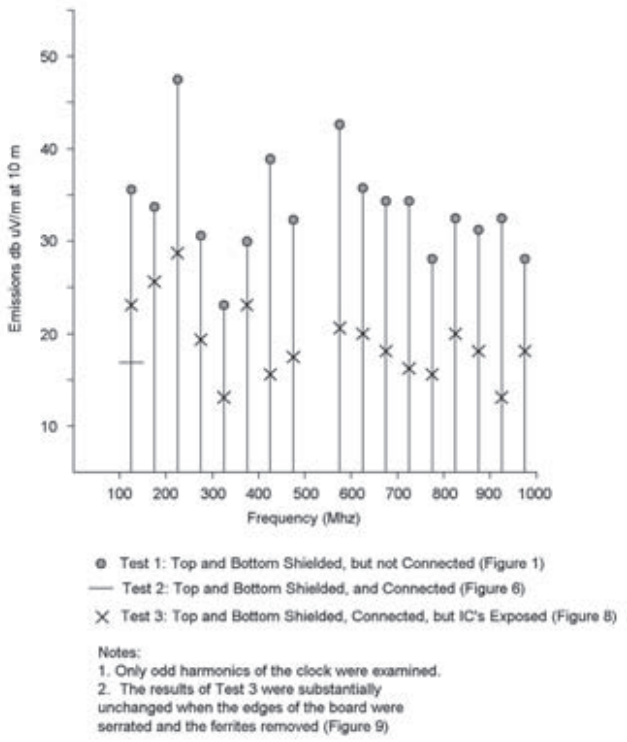

Figure 7: Our comparative emissions results.

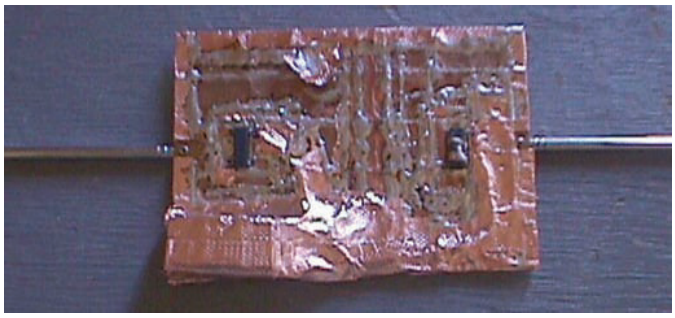

Figure 8: We modified the device by removing the shields over the ICs. Emission rose, but were still significantly lower than those detected from the device of Figure 1.

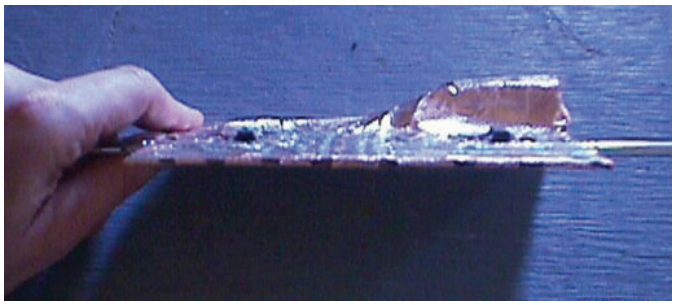

Figure 9: We serrated the edge of the fully shielded device of Figure 8. Emissions were not noticeably affected.

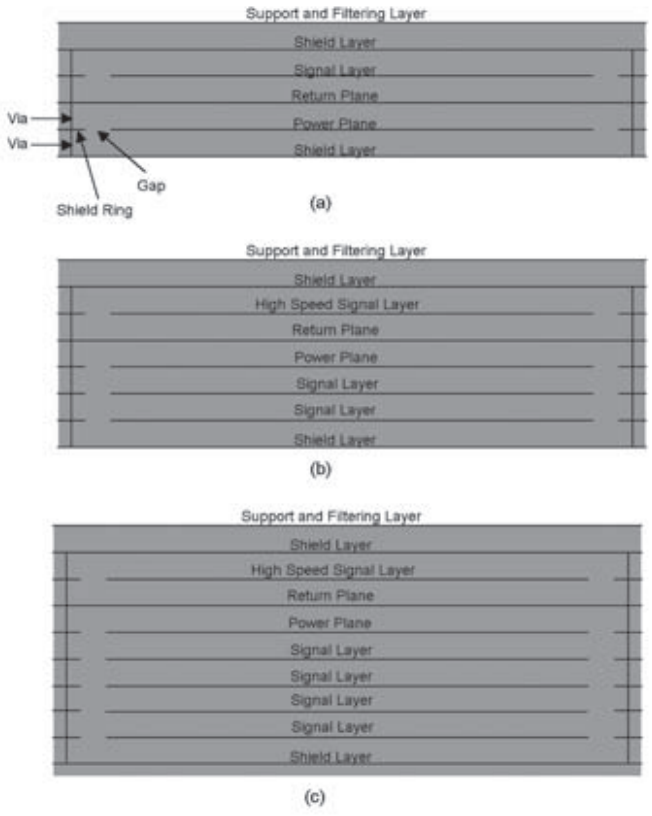

Figure 10: Some suggested stack ups.

The six layer stack up does not allow for much circuitry so the eight layer stack of Figure 10(b) may be more practical. Again, the top layer is used for component support and layers 2 and 8 comprise the shield. The outer centimeter or so of layers 3, 5, 6 and 7 are reserved for the shield rings. Vias passing through these rings connect the layers together, completing the shield. We have also chosen to make layer 4 a shield layer, isolating the high speed layer 3 from power layer 5.

A 10-layer stack up is also shown in Figure 10(c).

There are as many variations as there are combinations of circuit, power and shield layers, but all share a common theme. A shield is formed consisting of two of the outer layers of the PCB connected together at their edges through the use of shield rings and vias on the intervening layers

Note, however, that any conductors that exit this shield will radiate unless they are filtered or shielded. Fortunately, the

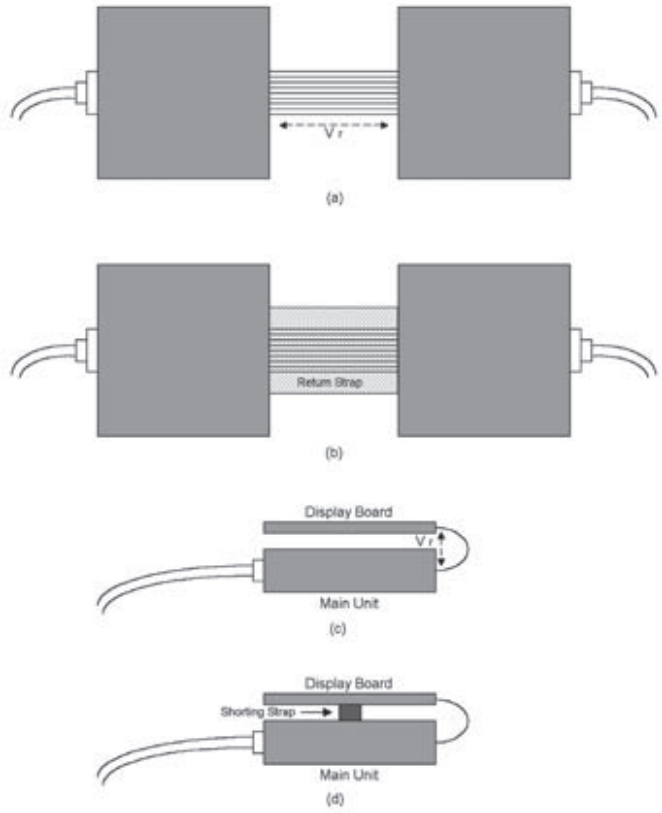

Figure 11: Even two well designed PCBs may radiate if interconnected with multi-conductor cable carrying high frequency currents. The inductance of the cable causes a voltage drop that drives the two PCBs and their attached I/O cables as if they were two halves of a dipole, even if they are shielded. A return strap can be used to "short out" V_r as shown in (b). Other designs can exhibit similar problems, but similar solutions can be employed as illustrated in (c) and (d).

support layer 1 and the shield layer adjacent to it are available to facilitate filtering and shielding.

Among the most challenging designs are those involving two or more PC boards (Figure 11). Let us assume that all the boards shown in Figure 11 have been properly designed as called for in this article. When interconnected they may still radiate badly. The problem is that the connection between the boards is inductive.

One solution is to provide a shorting strap as shown in Figure 11(b). While the connection between the two boards is inductive, the shorting strap essentially shorts out this voltage and greatly lessens radiation. To minimize its inductance, however, it must be nearly as wide as it is long.

Figure 11(c) shows a display board interconnected with a main unit, an arrangement common in notebook computers. I/O cables attached to the computer may radiate badly even if both the computer and the display board are well designed. The inductance of the cabling between them may be the culprit. It can cause a voltage drop between the display board and the main unit. This in turn causes the main unit and its attached I/O to act as one side of an antenna system and the display unit to act as its counterpoise. One solution is to short out the voltage source, V_r, with a short, fat shorting bar or strap as shown. ■

Glen Dash *is the author of numerous papers on electromagnetics. He was educated at MIT and was the founder of several companies dedicated to helping companies achieve regulatory compliance. Currently he operates the Glen Dash Foundation which uses ground penetrating radar to map archaeological sites, principally in Egypt. GlenDash@alum.mit.edu*

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