Introducing a new category of o

The 'n-chip' model for higher-power RF

The need for higher RF power means that functions which used to use a single component are now evolving into multi-component sub-systems changing the conventional, single-capacitor 'a-chip' model into the 'n-chip' model. **Charcroft** explores how this can be achieved with modern capacitors

The conventional approach to driving more power from an RF circuit is to move to a higher current, a higher voltage, or both. At some point, however, the physical limitations of a single capacitor reaches a point at which it is no longer possible to continue to increase the dielectric thickness or the number of electrodes. For example, a single capacitor can ensure the matching of a 100W RF transistor, however, the matching of the latest 1000W transistors needs to consider multiple capacitors, sometimes also with an increased capacitor size.

In order to understanding the demands of the n-chip model, designers need to consider the key parameters of high-power RF systems.

VOLTAGE RATING

The maximum voltage rating for a ceramic capacitor (WVDC) is linked to two factors: strength of the dielectric and Paschen's law. The strength of the dielectric provides a maximum voltage above which the capacitor breaks, as shown in Figure 1, whilst Paschen's law provides the maximum voltage above which the air around the chip arcs. The capacitor's voltage rating will be the lower of these two limitations.

For applications which need to operate at very high voltages, a coating, which covers both terminations of the capacitor can effectively eliminate the gap in which an electric arc could occur.

The current rating of a capacitor is stated in one of two ways: voltage-limited operation is directly proportional to the voltage rating and the impedance of the capacitor, whilst power-dissipation limited operation is directly proportional to the capacitor's ability to dissipate the heat and the Equivalent Series Resistance (ESR).

THE TRANSFER OF HEAT

The thermal properties of the capacitor are dependent on its ability to dissipate heat through thermal convection, thermal conductance, or thermal radiation. Thermal conduction contributes around 80% of the power dissipation, compared to 15% by convection and 5% by radiation. Therefore, the majority of heat is transferred through the capacitor's terminations. The use of non-magnetic micro-strip silver ribbons can improve the thermal path of a porcelain capacitor, in addition to acting as a mechanical strain relief when the thermal expansion coefficients of the capacitor and the PCB are mismatched.

Material	Dielectric Strength (kV/inch)
Vacuum	20
Air	20 to 75
Porcelain	40 to 200
Glass	2,000 to 3,000
Mica	5,000

Fig. 1: Comparison of dielectric strength

Capacitor Length	10.50	mm
Capacitor Width	9.50	mm
Capacitor Height	4.50	mm
Capacitor thermal resistance	10.23	°C/W
PCB thermal resistance	7.37	°C/W
Capacitor max operating temperature	125	°C
Ambient temperature	25	°C
Capacitance value	22	pF
Rated DC voltage	7000	V
Frequency	50.00	MHz
Duty Cycle	5	%
ESR @ Frequency	0.042	Ohm
The limitation is given by the	Voltage	
The maximum current is	34.210	Arms
The maximum voltage is	4 950	Vrms

Fig. 2: Example parameters to calculate the maximum current rating

THE GLOBAL POWER MODEL

A high-power RF design must factor-in the capacitor's electrical and thermal parameters, in addition to the properties of the PCB and the environment in which the complete system will operate. A simulation is used to calculate the maximum current rating of the capacitor, based on all the parameters in this global power model.

The example shown in Figure 2 is based on a single ceramic capacitor from Exxelia Temex's CLE series mounted onto a PCB. The capacitor has a capacitance value of 22pF, a voltage rating of 7000Vdc, and an operating frequency of 50MHz. The simulation calculates are for the voltage limitation (Iv) and the power limitation (Ip). The lower value represents the first limitation that the user will reach when using the system.

According to its power dissipation limitation, the capacitor in the example should handle around 52A (Ip) but the voltage limitation restricts its ability to handle more than 34A (Iv). If the capacitance function has to handle more current, then the n-chip model, shown in Figure 3, offers a solution.

PARALLEL COMBINATION

To effectively double the operating current, or to provide a further reduction in ESR, the designer should consider a parallel combination of ceramic capacitors. This also has the advantage of reducing ESR as 'n' capacitors in parallel will lead to an approximate reduction in ESR which is 'n'-times lower than for a single capacitor, therefore increasing the maximum current handling capability by a factor of 'n'.

To double the voltage rating, Hi-Q ceramic capacitors can be combined in series within the same dielectric die, or as separate capacitors. Finally, non-standard capacitance values, or ultra-tight tolerances can be achieved by using matched capacitors. Matched sets can also reduce the overall component costs by achieving a tight tolerance for the final assembly while using single chips which have a wider tolerance.

Other factors which can contribute to an increase in RF power are outlined in the technical paper, 'Power Capacitor Solutions: Ultra-low ESR, High RF Power' which is available on: www.charcroft.com/RFPower.

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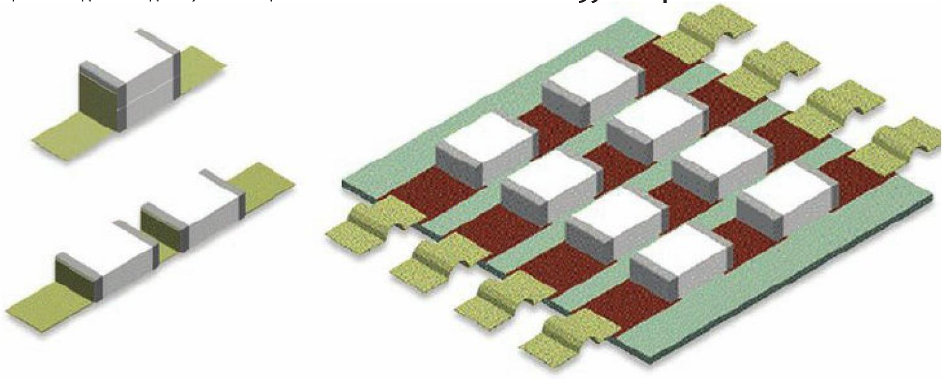

Fig. 3: In-chip configurations of ceramic capacitors: Parallel, series, matched sets