Senior Software Engineer for Edge AI Applications

Role specification: purpose, ownership, essential skills and desirable background

Salary: Competitive

Location: Ely, Cambridgeshire (a city repeatedly voted among the best places to live in the UK)

Employment Type: Full time, permanent

1. Role purpose

UBIETY Technologies Ltd requires a senior software engineer to develop the software stack for precision Edge-AI measurement instruments serving energy-transition, industrial and healthcare markets. Each instrument couples an analogue front end with a modern SoC-FPGA platform combining programmable logic (PL) with an embedded processing system (PS). The role works alongside an FPGA specialist, who owns the PL for deterministic timing, acquisition and high-rate data movement, and an algorithms engineer, who develops the measurement algorithms in MATLAB and Python. The software engineer owns the PS side of the PS–PL boundary: register maps, DMA buffers, interrupts, device tree, embedded Linux services for control, processing, diagnostics, industrial communication and user interaction, and the backend processing and user-facing interfaces. A central task is to translate the MATLAB/Python reference algorithms onto the PS — and, with the FPGA specialist, onto the PL. The three roles operate as a single team, and broader cross-disciplinary collaboration is expected and valued. Full details of our products and technology roadmap are shared at interview under confidentiality.

2. Primary ownership

Area	Expected ownership
Embedded Linux	Board software, Linux application services, boot/runtime configuration, logging, watchdogs and deployment.
PS–PL integration	AXI-Lite control, AXI DMA integration, DDR buffer management, interrupt handling, packet formats, deserialisation boundaries and PL bring-up tools.
Backend processing	Acquisition orchestration, waveform capture, diagnostic extraction, path health checks, flow-computation support and data persistence.
Industrial interfaces	Ethernet services, Modbus TCP register map, process-variable publishing, alarm/status words and configuration access.
User interface	Browser-based or desktop UI for commissioning, operation, calibration, diagnostics, event logs and service access.
Measurement integrity	Audit trail, protected calibration parameters, version traceability, configuration CRC, role-based access and controlled update/rollback.

3. Essential skills

Skill group	Required competence
Embedded Linux	Yocto or PetaLinux, U-Boot, kernel/device-tree awareness, systemd, cross-compilation, network configuration and field update strategy.
C/C++ backend	Modern C++ and C for low-level interfaces, multithreading, bounded queues, binary protocol handling, error handling, performance profiling and CMake/Make.
PS–PL interface	AXI-Lite, AXI-Stream, AXI DMA/CDMA, memory-mapped I/O, UIO/VFIO or kernel drivers, interrupts, cache coherency, contiguous buffers, serial-link bring-up and deserialised packet validation.
Signal processing & algorithm porting	ADC sample streams, filtering, FFT, cross-correlation, parameter estimation, interpolation, SNR, clipping, gain and channel diagnostics; translating MATLAB/Python reference algorithms into efficient, validated embedded C/C++.
Edge AI deployment	On-device inference of trained models on SoC-FPGA targets using vendor toolchains (e.g. Vitis AI/DPU) or equivalent runtimes: ONNX import, model quantisation and optimisation, fixed-point/integer pipelines and PS–PL partitioning of the inference workload.
Communications	Modbus TCP, TCP/IP sockets, REST/WebSocket APIs, register scaling, engineering units, endian handling and alarm/status design.
UI implementation	TypeScript with React/Vue/Svelte or equivalent, real-time charts, configuration screens, service pages, role-based access and waveform snapshots.
Quality discipline	Git, issue tracking, test automation, reproducible builds, logging, fault injection, diagnostics and release documentation.
Data & persistence	SQLite or time-series stores on embedded targets, ring buffers, log rotation, long-term onboard historical data retention and export formats (CSV/JSON/binary) for analysis tools.
Real-time & performance	Linux real-time tuning (PREEMPT_RT awareness), CPU affinity and thread priorities, latency measurement, zero-copy I/O and memory budgeting on resource-constrained embedded targets.
Build tooling & CI	Containerised cross-build environments (e.g. Docker), CI pipelines building and testing for embedded targets, artefact versioning, SBOM awareness and reproducible release packaging.

4. Desirable background

- SoC-FPGA platforms (e.g. AMD Zynq-class), industrial instrumentation, test-and-measurement systems.
- Medical or industrial imaging and reconstruction pipelines (e.g. ultrasound, MRI, CT).
- Edge AI/ML: Vitis AI tooling, model quantisation/pruning, TVM/TensorRT or equivalent, and hardware-aware optimisation of ML inference. Interest or experience in SciML such as PINNs/PIML as well as generic PyTorch/TensorFlow is a distinct advantage but not mandatory.
- Legal-metrology or other regulated-measurement environments: auditability, calibration locking, tamper evidence and secure device service access.
- OPC UA, MQTT, TLS/certificates, signed updates, A/B root filesystem deployment and factory-test automation.
- Python for hardware-in-the-loop test rigs, automated regression testing and measurement data analysis alongside MATLAB.

Employee benefits

- Modern, fully refurbished Ely offices; free parking; walking distance to Ely rail station
- 25 days annual leave + Bank Holidays, rising to 30 days with service
- Auto-enrolment workplace pension (optional, with opt-out under UK rules)
- Healthcare provided automatically, non-contributory
- 9am–5pm with one-hour lunch; role-based flexible/remote working day
- Cycle to Work scheme; supported team activities (e.g. staff rowing on the River Great Ouse)
- Performance-based share options after 3 years' employment