

Senior FPGA Engineer – Edge-AI Device

Role specification: purpose, ownership, essential skills and desirable background

Salary: Competitive

Location: Ely, Cambridgeshire (a city repeatedly voted among the best places to live in the UK)

Employment Type: Full time, permanent

1. Role purpose

UBIETY Technologies Ltd develops precision Edge-AI devices serving energy-transition, industrial and healthcare markets. Each device couples an analogue front end with a SoC-FPGA system-on-module: programmable logic (PL) plus an embedded processing system (PS). The Senior FPGA Engineer owns the PL and sits between the hardware engineer, who owns the boards and analogue front end, and the signal-processing and software engineers, who own the reference algorithms and the PS software. The work has a clear trajectory. Today, the fabric deserialises and frames multi-channel acquisition data and streams it by DMA to processor memory and onboard storage — an interim, data-gathering arrangement whose register, buffer and interrupt contract is designed and verified jointly with the software engineer. As the algorithms mature on that gathered data, the recorded-data path gives way to the destination architecture: on-the-fly processing in the fabric itself, with fixed-point reconstruction pipelines and CNN implementations of our foundational measurement models running at acquisition rate. Fabric designs ship as runtime-loadable overlays with Python drivers, validated from Jupyter notebooks such as via PYNQ or similar applications. The role therefore grows from high-rate data movement into real-time fabric DSP and CNN acceleration. Full details of our products and technology roadmap are shared at interview under confidentiality.

2. Primary ownership

Area	Expected ownership
Acquisition logic	Deterministic excitation and acquisition timing, multi-channel LVDS deserialisation, channel alignment, framing and streaming pipelines in the PL.
Data movement & storage	DMA engines streaming framed data into processor DDR and onboard high-rate storage during the data-gathering phase; buffer and throughput budgets agreed with the software engineer.
PS-PL contract	With the software engineer: register maps, interrupt/polling strategy, packet formats, buffer hand-off and bring-up tooling across bare-metal and embedded-Linux paths.
Hardware collaboration	With the hardware engineer: pin planning and constraints, clocking architecture, timing closure, and bring-up of new boards and modules.
Fabric DSP & Edge AI	The destination architecture: fixed-point filter, correlation and estimation blocks implemented from the algorithm engineers' MATLAB/Python references, and CNN implementations of foundational measurement models accelerated in fabric — processing on the fly at acquisition rate.
Platform stewardship	Fabric IP library curation, toolchain and constraint management, scripted builds, and assessment of design portability across FPGA families.
Verification & release	Self-checking testbenches, simulation regression, on-chip debug, versioned and scripted builds, and release documentation.

3. Essential skills

Skill group	Required competence
RTL design	Strong VHDL/Verilog/SystemVerilog; clock-domain crossing done correctly; timing constraints and closure; resource-aware coding for streaming pipelines.
SoC-FPGA integration	PS-PL interfacing on modern SoC-FPGA platforms: AXI-Lite/AXI-Stream/full AXI, DMA engines, interrupts, boot flow and bitstream/firmware co-loading.
High-speed interfaces	LVDS/source-synchronous deserialisation, DDR memory interfacing, PCIe fundamentals, and storage-path concepts including NVMe submission/completion queues.
Embedded software fluency	Bare-metal C drivers and embedded-Linux userspace/kernel interaction — enough to co-design and debug the PS-PL contract from both sides.
Clocking & synchronisation	Clock architecture for coherently sampled multi-channel acquisition: converter synchronisation, jitter awareness and deterministic-latency design.
DSP in fabric	Fixed-point arithmetic, filters, FFT and cross-correlation in hardware; throughput/latency/resource trade-offs; numerical validation against reference models.
Verification & debug	Simulation-first methodology, self-checking testbenches, on-chip logic analysis, and hardware-in-the-loop validation against specification.
Overlay & Python workflow	Packaging fabric designs as runtime-loadable overlays with Python drivers; Jupyter-driven bring-up, validation and data capture.
Quality discipline	Git-based HDL workflow, scripted/reproducible builds, issue tracking, design documentation and disciplined release practice; SCRUM-based teamwork.

4. Desirable background

- Major-vendor SoC-FPGA system-on-module platforms and toolchains (e.g. AMD/Xilinx, Intel/Altera).
- CNN inference acceleration in fabric (vendor accelerator IP or custom pipelines); training or deploying CNNs/foundation models on imaging or physical-measurement data; quantisation-aware design.
- Vendor-portable RTL practice and interest in open/portable toolchains.
- Multi-channel instrumentation or ultrasound/imaging front ends; mixed-signal board bring-up; EMC-aware digital design.

Employee benefits

- Modern, fully refurbished Ely offices; free parking; walking distance to Ely rail station
- 25 days annual leave + Bank Holidays, rising to 30 days with service
- Auto-enrolment workplace pension (optional, with opt-out under UK rules)
- Healthcare provided automatically, non-contributory
- 9am–5pm with one-hour lunch; role-based flexible/remote working day
- Cycle to Work scheme; supported team activities (e.g. staff rowing on the River Great Ouse)
- Performance-based share options after 3 years' employment