Senior Software Engineer for Edge AI Applications

Role specification: purpose, ownership, essential skills and desirable background

(ca. £55K)

1. Role purpose

UBIETY Technologies Ltd requires a senior software engineer to develop the software stack for industrial Edge AI devices such as multiphase flow meters and medical imaging instruments. Each instrument couples an analogue front end with an AMD Zynq UltraScale+ MPSoC. The role works alongside an FPGA specialist, who owns the programmable logic (PL) for deterministic timing, acquisition and high-rate data movement, and a Signal Processing and Tomography engineer, who develops the reconstruction and flow algorithms in MATLAB and Python. The software engineer owns the processing system (PS) side of the PS–PL boundary: register maps, DMA buffers, interrupts, device tree, embedded Linux services for control, processing, diagnostics, industrial communication and user interaction, and the backend processing and user-facing interfaces. A central task is to translate the MATLAB/Python reference algorithms onto the PS — and, with the FPGA specialist, onto the PL — covering acquisition orchestration, waveform capture, diagnostic extraction, path health checks, flow-computation support and data persistence. The three roles operate as a single team, and broader cross-disciplinary collaboration is expected and valued.

2. Primary ownership

Area	Expected ownership
Embedded Linux	Board software, Linux application services, boot/runtime configuration, logging, watchdogs and deployment.
PS–PL integration	AXI-Lite control, AXI DMA integration, DDR buffer management, interrupt handling, packet formats, deserialisation boundaries and PL bring-up tools.
Backend processing	Acquisition orchestration, waveform capture, diagnostic extraction, path health checks, flow-computation support and data persistence.
Industrial interfaces	Ethernet services, Modbus TCP register map, process-variable publishing, alarm/status words and configuration access.
User interface	Browser-based or desktop UI for commissioning, operation, calibration, diagnostics, event logs and service access.
Custody-transfer integrity	Audit trail, protected calibration parameters, version traceability, configuration CRC, role-based access and controlled update/rollback.

3. Essential skills

Skill group	Required competence
Embedded Linux	Yocto or PetaLinux, U-Boot, kernel/device-tree awareness, systemd, cross-compilation, network configuration and field update strategy.
C/C++ backend	Modern C++ and C for low-level interfaces, multithreading, bounded queues, binary protocol handling, error handling, performance profiling and CMake/Make.
PS–PL interface	AXI-Lite, AXI-Stream, AXI DMA/CDMA, memory-mapped I/O, UIO/VFIO or kernel drivers, interrupts, cache coherency, contiguous buffers, serial-link bring-up and deserialised packet validation.
Signal processing & algorithm porting	ADC sample streams, filtering, FFT, cross-correlation, time-of-flight estimation, interpolation, SNR, clipping, gain and path diagnostics; translating MATLAB/Python reference algorithms into efficient, validated embedded C/C++.
Edge AI deployment	On-device inference of trained models on the MPSoC: Vitis AI/DPU or equivalent runtimes, ONNX import, model quantisation and optimisation, fixed-point/integer pipelines and PS–PL partitioning of the inference workload.
Communications	Modbus TCP, TCP/IP sockets, REST/WebSocket APIs, register scaling, engineering units, endian handling and alarm/status design.
UI implementation	TypeScript with React/Vue/Svelte or equivalent, real-time charts, configuration screens, service pages, role-based access and waveform snapshots.
Quality discipline	Git, issue tracking, test automation, reproducible builds, logging, fault injection, diagnostics and release documentation.

4. Desirable background

- AMD Zynq UltraScale+ MPSoC, industrial instrumentation, test-and-measurement systems.
- Tomographic reconstruction or medical/industrial imaging pipelines (ultrasound, MRI, CT).
- Edge AI/ML: Experience in Edge AI tooling Vitis AI, model quantisation/pruning, TVM/TensorRT or equivalent, and hardware-aware optimisation of ML inference. Interest or experience in SciML such as PINNs/PIML as well as generic PyTorch/TensorFlow is a distinct advantage but not mandatory.
- Custody-transfer, legal-metrology, auditability, calibration locking, tamper evidence and secure device service access.
- OPC UA, MQTT, TLS/certificates, signed updates, A/B root filesystem deployment and factory-test automation.