DEVELOPMENT OF UVM VERIFICATION TESTBENCH FOR SUPERSPEED USB DUAL ROLE SUBSYSTEM

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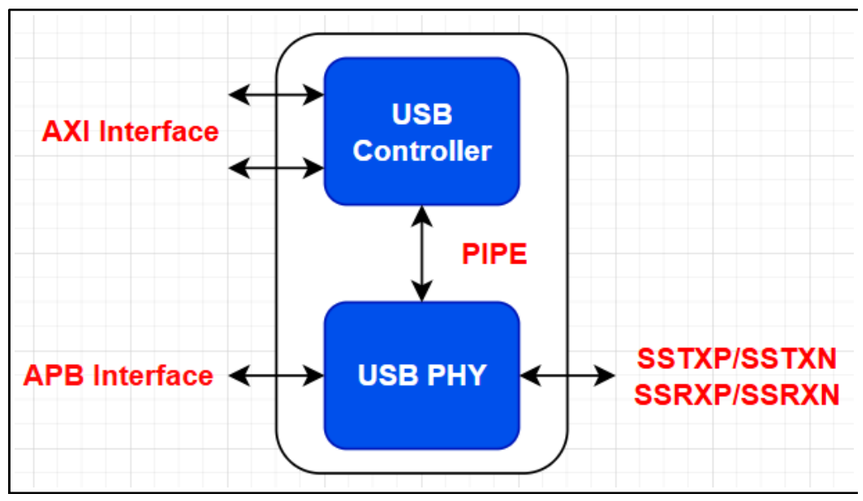
Project Description

- The primary role of the testbench is to guarantee the subsystem's reliability by thoroughly inspecting the communication channel, including both logical pathways and data transfers, that connects the USB 3.2 controller with the PHY, confirming its correct operation in both Host and Device modes.

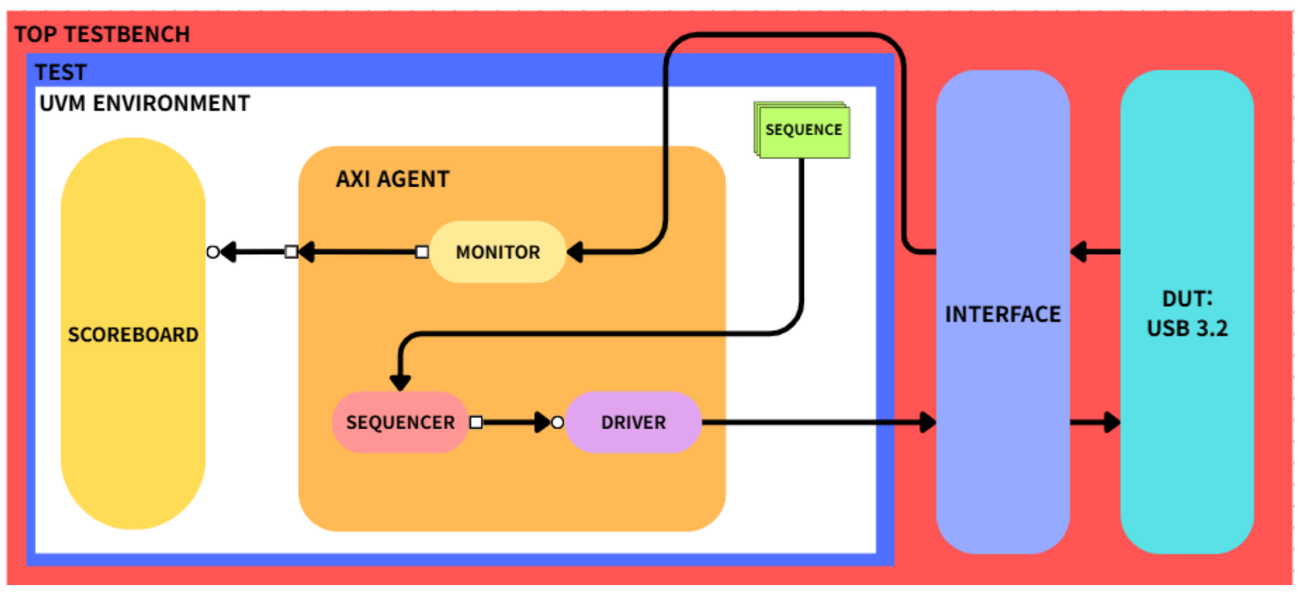
- By verifying compliance with the official USB 3.2 protocols and conducting thorough testing, the team aims to guarantee that the subsystem meets all stated requirements. The goal is to ensure it operates correctly and reliably within both Host and Device modes, confirming its readiness for system integration and deployment.

USB Subsystem Overview



Faraday USB 3.2 Subsystem

Design Methodology



- Build a UVM-based testbench, which is a reusable verification environment to enable effective communication between the testbench and DUT.

- Implement AXI protocols to request entry and exit low power state of USB subsystem.

- Integrate Synopsys USB 3.2 VIP into the testbench to ensure proper communication protocols with the DUT.

- Develop the testbench using SystemVerilog, constructing its structure following a bottom-up hierarchy approach.

Verification Results

dut_device_ss_u1_vip_init_dut_exit.228947.vcs	Pass
dut_device_ss_u1_dut_init_vip_exit.225347.vcs	Fail
dut_host_ss_u1_dut_init_dut_exit.210861.vcs	Pass
dut_device_ss_u1_vip_init_vip_exit.279476.vcs	Fail
dut_host_ss_u1_vip_init_dut_exit.947253.vcs	Pass
dut_device_ss_u1_dut_init_dut_exit.145527.vcs	Pass

dut_host_ss_u2_entry_exit.280821.vcs	Fail
dut_host_ssp_u1_dut_init_vip_exit.474689.vcs	Pass
dut_host_ssp_u1_vip_init_vip_exit.308965.vcs	Pass
dut_device_ssp_u1_vip_init_vip_exit.341129.vcs	Pass
dut_host_ssp_u1_vip_init_dut_exit.43818.vcs	Fail
dut_device_ssp_u1_dut_init_vip_exit.232378.vcs	Pass