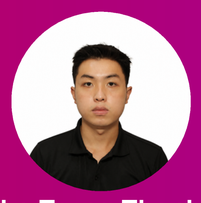
8Gb/s Analog Front-End Receiver Chip for Die-to-Die Links in Data Center


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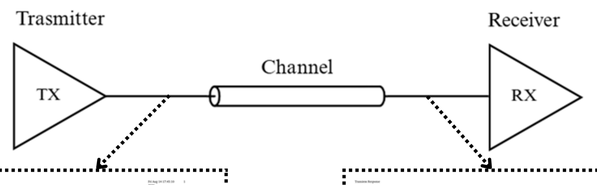
Industry Supervisor

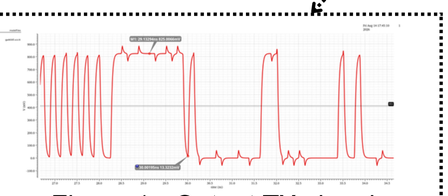
Mr. Le Van Quyen (Synopsys)

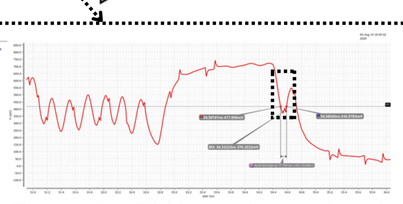
Mr. Chuong Quoc Tin (Synopsys)

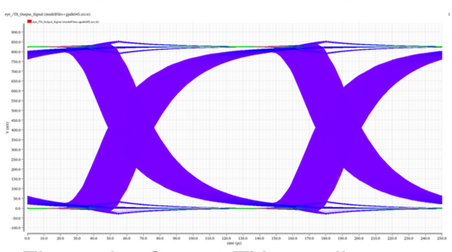
Motivation

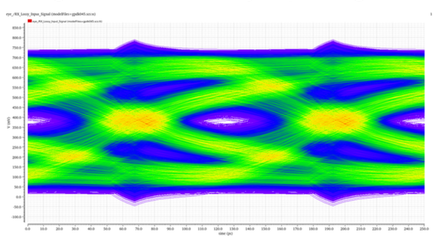
The increasing demand for high-performance AI computing requires data center to process information at ever-faster speed. Within each server, multiple dies inside a single chip package must communicate with one another at high speed to keep pace with these processing demands. However, as data rates increase, channel loss in this die-to-die link causes TX signal (figure 1) attenuation and inter-symbol interference (ISI) at the receiver side (figure 2).




Figure 1 - Output TX signal


Figure 2 - RX lossy input signal

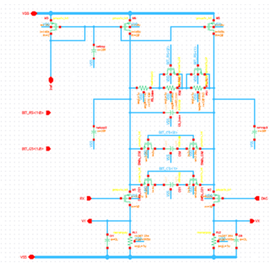

Figure 3 - Output TX eye diagram

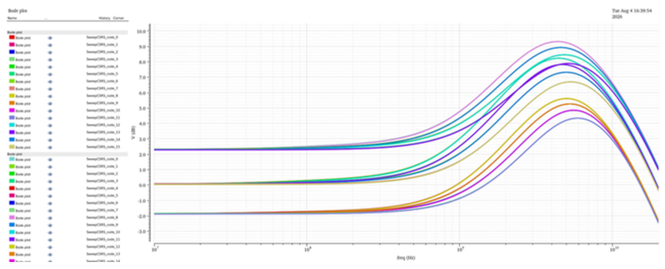

Figure 4 - RX lossy input eye diagram

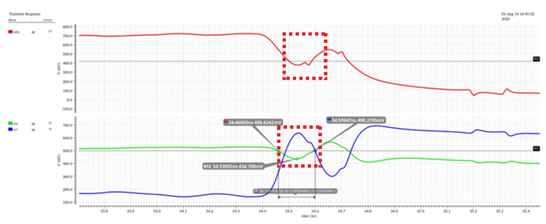
The bit affected by ISI, marked in figure 2 drops only 39 (mV) below the offset and remains there for just 83 (ps). This is too short for the comparator block to reliably detect it as a 0, since a minimum timing budget is required correctly sample the bit.

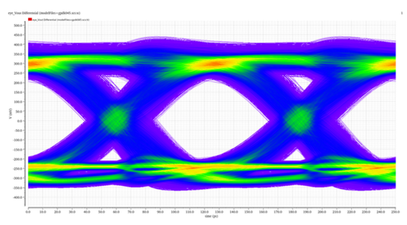
Programmable CTLE Design

To boost amplitude and reduce ISI, a 4-bit Programmable CTLE (figure 5) provides peaking gains of 4 - 10 (dB) and peaking frequency of 4 - 6 (GHz) (figure 6). This not only improves the margin below the offset from 39 (mV) to 63 (mV) and extends the timing budget from 83 (ps) to 139 (ps) (figure 7), opening the eye diagram (figure 8) for correct comparator detection, but also improves flexibility for different channel losses.


Figure 5 - Prog CTLE schematic


Figure 6 - Full AC frequency response tuning range

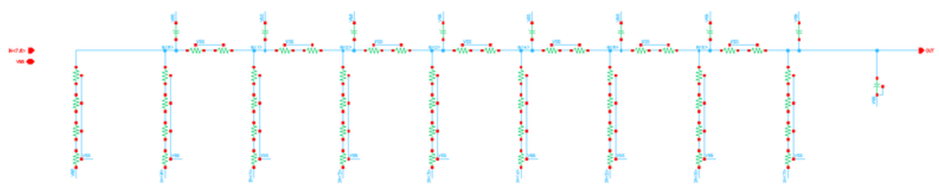

Figure 7 - CTLE output transient shows ISI reduction


Figure 8 - CTLE output eye diagram

In the same context, as channel characteristics vary, the DC voltage of the RX input signal also shifts. Using a fixed reference voltage for the input CTLE then causes an unbalanced signal swing at the output. To adapt to different input offset voltage, a DAC is designed to generate a programmable reference voltage for CTLE.

DAC Design

A Digital-to-Analog Converter transforms binary codes into analog signals (output voltages). To meet the system requirements of low power consumption, an R-2R - based DAC (RDAC) (figure 9) was selected. In this design, the DAC accepts an 8-bit input and provides output range of 0 to 1.2 V. Both DNL and INL remain within ±0.5 LSB (figure 10 - 11), while the current consumption at code 255 is 61.72 uA.


Figure 9 - R-2R resistor-based DAC

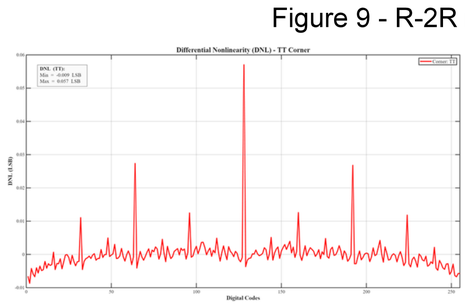


Figure 10 - DNL

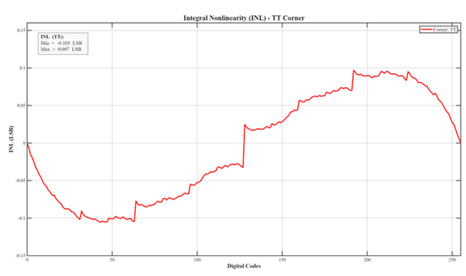
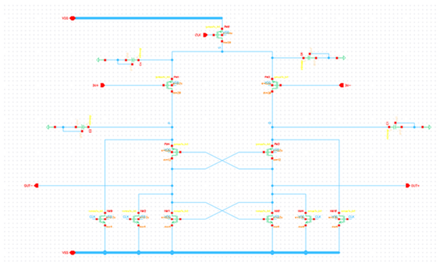


Figure 11 - INL

Comparator Join In - Bit Detected Correctly?


Figure 12 - StrongARM schematic

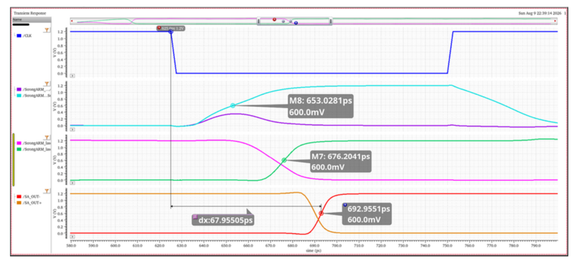


Figure 13 - StrongARM Delay Simulation at TT Corner

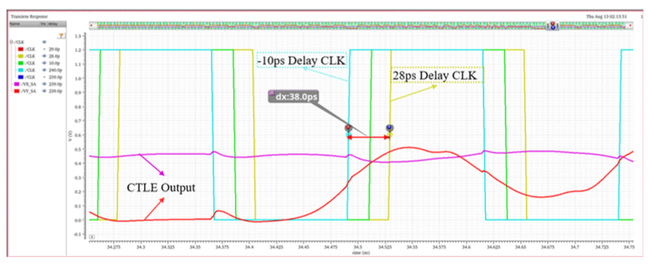
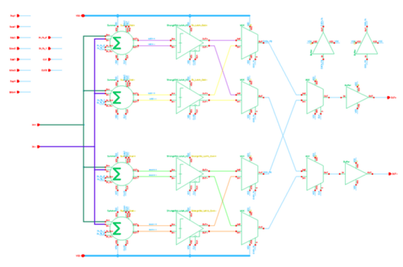


Figure 14 - StrongARM–CTLE Transient Response Under Clock Phase Shift

The StrongARM comparator (figure 12) was selected for this design due to its rail-to-rail output capability. Simulation results show a 67.9 (ps) delay at the TT corner (figure 13), providing sufficient timing margin for 8 (Gb/s) operation.

The CLTE output was then directly connected to the StrongARM. Transient simulations show that this architecture can tolerate 38 (ps) of clock phase shift while maintaining correct bit detection (figure 14). This result highlights the inherent timing sensitivity of the receiver, motivating the proposed loop-unrolled DFE architecture to extend the allowable timing window.

DFE Design


Figure 15 - Loop-Unrolled DFE Architecture

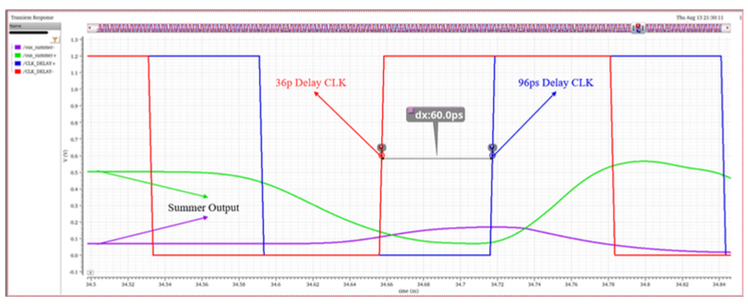
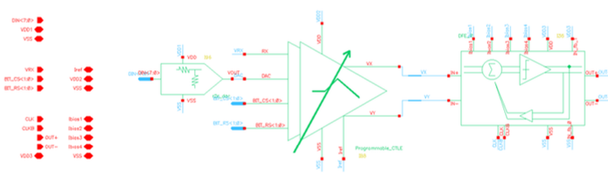


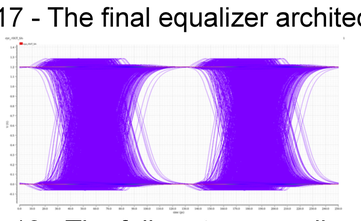
Figure 16 - DFE Timing Response Under Clock Phase Shift

The loop-unrolled DFE architecture (figure 15) is selected to relax the stringent timing requirements of the feedback loop. Integrating the CTLE and DFE extends extend the allowable clock timing variation from 38 (ps) to 60 (ps) (figure 16), significantly improving timing margin to detect bit correctly.

Final Equalizer Architecture

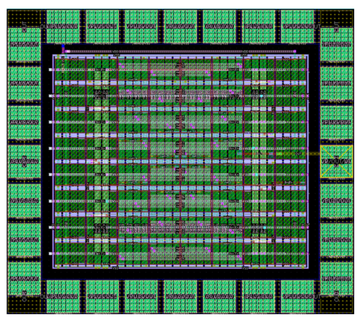
The final equalizer architecture (figure 17) includes a 4-bit Programmable CTLE, an 8-bit DAC, and a loop-unrolled DFE (Summer + StrongARM + SR latch), which detects the bit correctly and opens the full rail-to-rail eye diagram (figure 18).


Figure 17 - The final equalizer architecture


Figure 18 - The full system eye diagram

Layout

All three core blocks (DAC, CTLE, and DFE) were laid out (figure 19, 20, 21) using several matching techniques including common-centroid, dummy device, and guard rings. These blocks are clean of DRC, LVS and ready for post-layout simulation.


Figure 19 - DAC layout

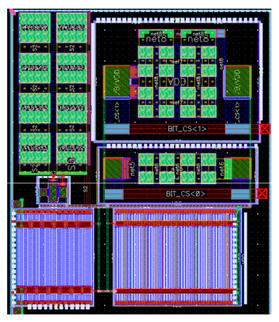
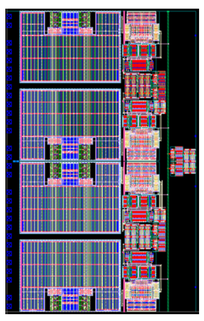
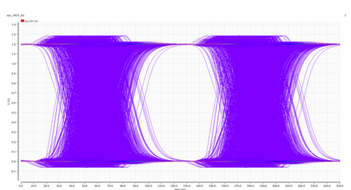


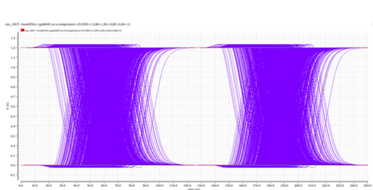
Figure 20 - CTLE layout


Figure 21 - DFE layout

Post-Layout

The RC parasitics of the full system layout were extracted to re-run the eye diagram. The post-layout eye diagram (figure 23) shows slightly higher jitter and ISI than pre-layout eye diagram (figure 22), but all bits are still detected correctly.


Figure 22 - Pre-layout eye diagram


Figure 23 - Post-layout eye diagram