LOW NOISE LOCAL OSCILLATOR FOR 5G TRANSCEIVERS

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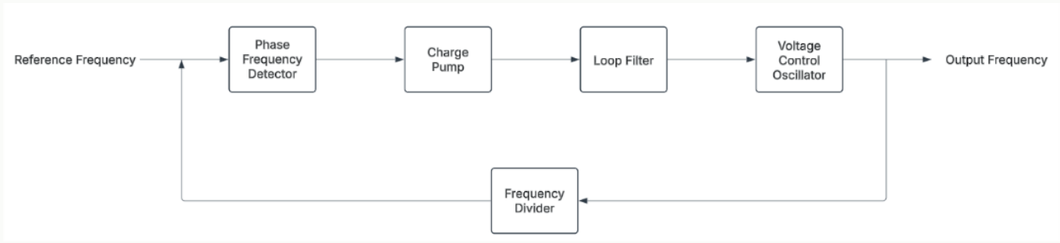
BACKGROUND & MOTIVATION

Modern 5G communication systems rely on precise and stable signals to transfer huge amounts of data at very high speeds. At the heart of this lies the local oscillator (LO), which generates the high-frequency signals used in smartphones, base stations, and wireless networks. To achieve this, advanced phase-locked loop (PLL) circuits are essential, ensuring accuracy, low noise, and energy efficiency. This project develops a next-generation PLL-based LO to meet 5G's demanding requirements for speed, reliability, and compact design.
The target specifications are listed as follows:

- Fundamental frequency > 26 GHz
- RMS noise jitter < 150 fs
- Power consumption < 30 mW
- Active area < 0.4 mm^2

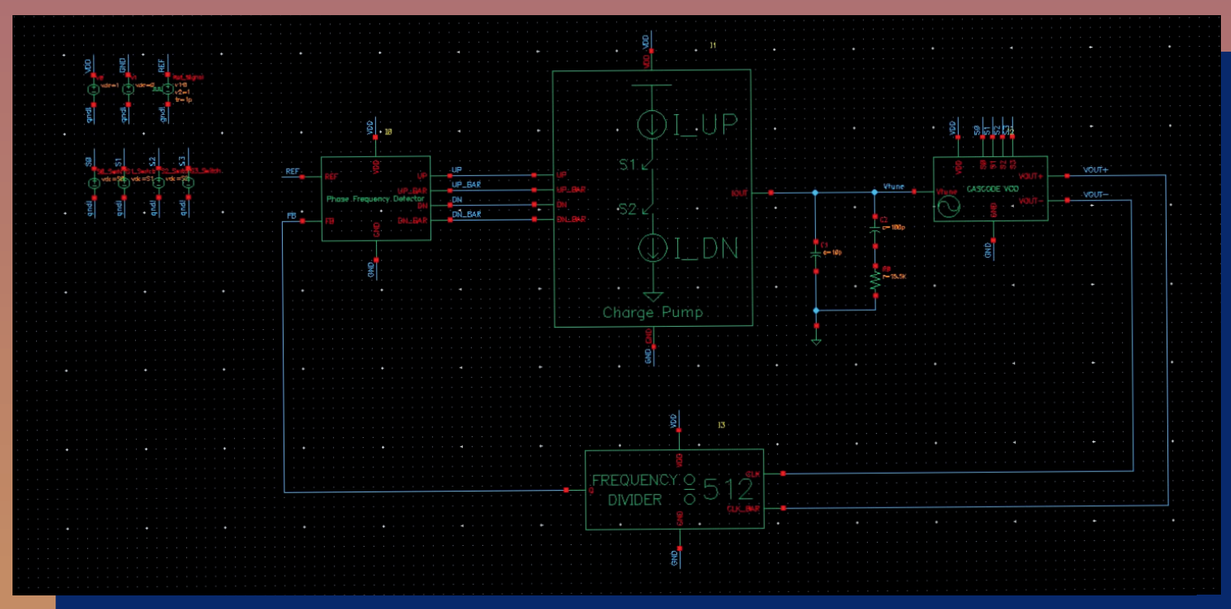


METHODOLOGY

Topologies of the blocks must carefully be chosen that match our knowledge and design capabilities while still aiming to meet the strict requirements of 5G systems as closely as possible. This involves making careful trade-offs – optimally balancing jitter, power consumption, chip area, and design complexity – so that the final design remains both achievable and effective.

Design process is as follow:

- Design each block using references from existing topologies except the VCO.
- Test functionality, analyze phase noise, and power consumption.
- Place and route components to minimize active chip area.
- Run PVT variation tests and parasitic extraction to confirm reliability and performance.



CONCLUSION

- Successfully designed and tested the topologies of each PLL block, including performance analysis of phase noise and power consumption.
- Managed to layout all blocks, ensuring optimized placement and routing to minimize active chip area.
- Developed a novel VCO topology as part of the design, contributing to improved performance in the overall PLL.

EXPERIMENTAL RESULTS