FPGA Conference EUROPE

Program 2025

3 Days – 9 Thematic Focus Tracks – 100 Percent Knowhow

organized by ELEKTRONIK PRAXIS PLC2

Tuesday, July 1

8:20 - 8:30 am — Welcome Session: Stefan Krassin | plc2 GmbH & Maria Beyer-Fistrich | Vogel Communications Group GmbH & Co. KG

8:30 - 8:55 am — OPENING SPEECH: Powering the Future – How Low Power FPGAs are Shaping Tomorrow's Tech Landscape | Pravin Desale - Lattice Semiconductor

	Application	Language / Debug / Verification	Architecture	Safety & Security	AI / ML	Tutorials
9:00 am - 10:30 am	Ansgar Hein - SGET **HFM – The First Open FPGA Standard is Taking Shape** (40 min)	Salma Hamdoun - Arrow Central Europe GmbH **FPGA Verification and Testing** (40 min)	Stefan Unrein - plc2 Design GmbH **Firmware Architecture for FPGAs** (40 min)	Marco Höfle - Avnet EMG AG **Welcome to the Post-European Cyber Resilience Act (CRA) Era** (90 min)	Alexander Flick - plc2 GmbH **Vitis AI for Versal AIE-ML and Versal AI Edge Series Gen 2** (40 min)	Eugen Krassin - plc2 GmbH **Design of an UART** (90 min)
	Jan Sigg - Emerson **Efficient FPGA Development and Beyond** (40 min)	Stefan Unrein - plc2 Design GmbH **Live Design Investigation** (40 min)	Prof. Dr. Markus Pfaff - FH Oberösterreich Studienbetriebs GmbH **Don't! - Frequently Encountered FPGA Design Quirks you Better Avoid** (40 min)		Yashwant Dagar - Intelligent Edge Systems **Automating FPGA System Design Using Generative AI Agents Within Xilinx Vivado IP Integrator** (40 min)	
10:30 - 11:15 am	Coffee break					
11:15 am - 12:45 pm	Patrick Lehmann & Stefan Unrein - plc2 Design GmbH **The PoC Library - Open-Source VHDL Component Library "Pile of Cores"** (40 min)	Jim Lewis - SynthWorks Design Inc **Getting Started with OSVVM** (40 min)	Oren Hollander - HandsOn Training **The Next Generation SoC FPGAs is Here!** (40 min)	Roger May - AMD **FPGAs and the Cyber Resilience Act** (40 min)	Gianluca Mariani - Lattice Semiconductor **Designing AI Solutions with Lattice for Real World Applications** (40 min)	Eugen Krassin - plc2 GmbH **Design of an SPI CONTROLLER to Control External DACs** (90 min)
	Patrick Lehmann & Stefan Unrein - plc2 Design GmbH **The PoC Library - Open-Source Universal AXI4-Lite Register** (40 min)	Jim Lewis - SynthWorks Design Inc **OSVVM, the New And More Recent Updates** (40 min)	Marco Smutek - Knowledge Resources GmbH **Key Criteria for Choosing an RFSoM** (40 min)	Martin Kellermann & Brian Colgan - Microchip Technology **Cyber Resilience Act: Planning your Security Future** (40 min)	Christian Michel - Lattice Semiconductor **Deploying Edge AI Applications with Lattice sensAI AI Solution Stack** (40 min)	
12:45 - 1:30 pm	Lunch break					
1:30 - 2:00 pm	KEYNOTE SPEECH: Edge AI Everywhere: How Platforms Can Reap Efficiency Benefits | Michael Hutchison - AMD					
2:00 - 2:15 pm	Short break					
2:15 pm - 3:45 pm	Thomas Kuhn - HTV Halbleiter-Test & Vertriebs-GmbH **It's not too late! From Component Testing, Quality Analysis and Component Preparation to Long-Term Preservation** (40 min)	Espen Tallaksen - EmLogic AS **Making Simple FPGA Testbenches – Utilising Important Quality Measures** (40 min)	Aniket Kolarkar - AMD **What's in a Name: FPGA vs. Adaptive SoC** (40 min)	Prof. Asaad Nayyef - ASMY Software Group **Next-Generation Cybersecurity Strategic Shielding for Fortifying EU Infrastructures** (40 min)	Joachim Müller - Efinix GmbH **Mix and Match – FPGA-Based AI Inference and Acceleration Using Quad Core RISC-V** (40 min)	Eugen Krassin - plc2 GmbH **Design of an SPI CONTROLLER to Control an External ADC** (90 min)
	Kleanthis Papachatzopoulos - CAST Inc. **A Cuckoo Hash-Based CAM Architecture for FPGA and ASIC Implementations** (40 min)	Espen Tallaksen - EmLogic AS **FPGA Requirements Tracking and the Requirements Traceability Matrix** (40 min)	Alexander Flick - plc2 GmbH **Versal Adaptive SoC Family: Adding Versal AI Edge Series Gen 2** (40 min)	Valtteri Allekotte - Xiphera Ltd. **Building a Secure System Leveraging FPGA-Based Hardware Root-of-Trust and Secure Boot** (40 min)	Martin Kellermann & Brian Colgan - Microchip Technology GmbH **Low-Power, High-Performance AI on Microchip FPGAs** (40 min)	
3:45 - 4:30 pm	Coffee break					
4:30 pm - 6:00 pm	Tomas Thoresen - AMD **The Right Engine for the Right Task: How to Achieve Real-Time, Determinism, and Mixed-Criticality in Robots** (40 min)	Gabriel Chidolue - Siemens EDA **Acceleration Techniques for FPGA Simulation and Debug** (40 min)	Romisaa Samhoud - AMD **Elevate your Design: Security and Power Efficiency with AMD Spartan UltraScale+ FPGAs** (40 min)	Yosri Jlassi - Arrow Central Europe GmbH **From Bit Flips to Bulletproof: Radiation Hardening in FPGA Technology** (40 min)	Hanni Lozano - SiWave Semiconductor Corporation **ML Inference Compiler for FPGAs** (40 min)	Eugen Krassin - plc2 GmbH **Band Pass Design** (90 min)
	Martin Kellermann & Brian Colgan - Microchip Technology GmbH **The Robot Revolution** (40 min)	Patrick Lehmann - plc2 Design GmbH **Let's Use VHDL-2019** (40 min)	Nikolai Krassin - plc2 GmbH **Faster Change of Probe Signals using the Vivado Logic Analyzer** (40 min)	Dr. Hassan Nassar - Karlsruhe Institute of Technology (KIT) **Mitigating Fault Injection Attacks in Multi-Tenant FPGAs: Detection and Response Mechanisms** (40 min)	Alexey Lopich - Altera **Intelligent Cameras: AI-Infused Image Signal Processing** (40 min)	
from 7:00 pm	Evening Event @ Motorworld Inn in Munich sponsored by AMD					

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Wednesday, July 2

	Application	Language / Debug / Verification	Embedded / Vision	Tools & Methodologies	Safety & Security	Tutorial
9:00 am - 10:30 am	Nikolai Krassin - plc2 GmbH **101 – Timing Closure** (40 min)	Mariano Olmos Martín - INDRA SISTEMAS SA **Mixed Verification: Regression Simulation Testbench with UVM for RTL Modules in VHDL** (40 min)	Jens Michaelsen - Avnet Silica & Ernst Wehlage - plc2 GmbH **MicroBlaze V Now! - The Way to Run RISC-V on AMD Hardware** (90 min)	Jasvinder Khurana - AMD **Integrating Adaptive Computing in Robotics: A Deep Dive into the AMD Kria Robotics Stack** (40 min)	Oren Hollander - HandsOn Training **Warning! Your FPGAs & SoC FPGAs are Under Attack** (40 min)	Jim Lewis - SynthWorks Design Inc **OSVVM's Test Reports and Requirements Tracking** (90 min)
	Nikolai Krassin - plc2 GmbH **Circuit Design** (40 min)	Kamil Rudnicki - Brightelligence sp. z o.o. **FPGA Design Debugging... How Hard Can It Be?** (40 min)		Derek Hagen - AMD **Vitis Functional Simulation: A Unified Framework for AI Engine and HLS Design Validation** (40 min)	Martin Kellermann - Microchip Technology & Nikola Velinov - Green Hills Software **Functional Safety for Hardware and Software** (40 min)	
10:30 - 11:15 am	Coffee break					
11:15 am - 12:45 pm	Niek van Agt & Dirk van den Heuvel - TOPIC Embedded Systems **Breaking the Electron-Photon Barrier Using FPGA technology** (40 min)	Prof. Dr. Torsten Reuschel - University of New Brunswick **CAVEAT – An Open-Source Framework for Context-Aware Verification, Emulation, and Training** (40 min)	Tolga Sel - Arrow Central Europe GmbH **Introduction to the HPS Architecture and Tutorial on How to Build and Run Linux on an Agilex 5** (40 min)	Tom Richter - The MathWorks GmbH & Maximilian Werner - Efinix GmbH **Empowering Designers: From MATLAB to Efinix FPGA** (40 min)	Matthias Lai & Harald Friedrich - NewTec GmbH **Security, Regulations and FPGA-Based Systems – How to Make Your System Secure** (40 min)	Jim Lewis - SynthWorks Design Inc **Development of a Wishbone Verification Component with OSVVM** (90 min)
	Nory Nakhaee - Sundance DSP **Enabling Space Missions** (40 min)	Hans-Jürgen Schwender - Var Group **Maximizing Early Bug Detection with a Static and Advanced Linting Solution in a CI Flow** (40 min)	Alexey Lopich - Altera, an Intel Company **DSP Block Based Soft-Processor FPU Design** (40 min)	Timo Osterkamp - Sokratel GmbH & Baruch Mitsengendler - The MathWorks GmbH **Model-Based Design (MBD) for Intelligent Field Devices in Industrial Automation** (40 min)	Jonathan Graf - Graf Research Corporation **Verify the Bits that Fly : A Demonstration of Bitstream to HDL Equivalence Checking** (40 min)	
12:45 - 1:30 pm	Lunch break					
1:30 - 2:00 pm	**KEYNOTE SPEECH: Learn About Altera's Strategy and Commitment in the FPGA Market | Ilya Ganusov - Altera, an Intel Company**					
2:00 - 2:15 pm	Short break					

	Application	Language / Debug / Verification	Embedded / Vision	Tools & Methodologies	Board Design & Connectivity	Tutorial
2:15 pm - 3:45 pm	Patrick Lehmann & Navid Jalali | plc2 Design GmbH **Bugs, Bugs, Bugs, Everywhere Bugs - What We Have Seen in Real World Projects** (40 min)	Oliver Bründler - Enclustra GmbH **Introduction to the VUnit Verification Framework** (40 min)	Prof. Dr. Bernhard Lang - Hochschule Osnabrück **A Fine-Grained Multi-Threading RISC-V for FPGA Systems** (40 min)	Dr. Hardik Shah - Lattice Semiconductor **Tools and Techniques for Higher Design Efficiency** (40 min)	Baruch Mitsengendler - The MathWorks GmbH **When FPGAs Meet System Engineering** (40 min)	Espen Tallaksen - EmLogic AS **FPGA Verification Architecture – The Key to Checking the Design Quality in an Efficient and Reusable Manner** (90 min)
	Oren Hollander - HandsOn Training **Area & Power Reduction: Can You Beat The Synthesizer?** (40 min)	Michal Pacula - Aldec **Why VUnit?** (40 min)	Fabian Heinrici - Efinix GmbH **Efinix RISC-V Solutions from Soft to Hard** (40 min)	Hoon Choi - Lattice Semiconductor **Open Standard Based High-Level Design Methodology for Near-Sensor Low-Latency Computing** (40 min)	Andreas Günther - SiTime **Driving Next-Gen FPGA Performance: How MEMS Timing Powers Data Center, AI, and Industrial Innovation** (40 min)	
3:45 - 4:30 pm	Coffee break					
4:30 pm - 6:00 pm	Davide Cieri - Max Planck Institute for Physics **Managing and Versioning Gateware Source Code on Git with Hog** (40 min)	Markus Leiter - P2L2 GmbH **Enhancing FPGA Verification by Combining VUnit and UVVM** (40 min)	Stefan Garcia - Altera, an Intel Company **RISC-V FPGA Soft Processor Implementations** (40 min)	Marc Schäfers - Eccelerators GmbH **Reimagining FPGA Design: The Impact of Higher-Level Languages and AI** (40 min)	Noritaka Chiyo & Herman Neufeld - TDK **Practical Power Designs for New FPGA/SoCs** (40 min)	Espen Tallaksen - EmLogic AS **The Important Mechanisms to Assure a Good FPGA Quality Through Efficient Simulation** (90 min)
	Patrick Lehmann & Navid Jalali - plc2 Design GmbH **A Baseboard Management Controller for FPGA/SoC Board Supervision and Faster Bringup** (40 min)	Oliver Bründler - Open Logic **Open Logic – Open-Source FPGA Standard Library** (40 min)	Karl Wachswender - Lattice Semiconductor **Adaptive RISC-V SoC for Industrial Edge AI Using Low power FPGA** (40 min)	Dr. Harald Simmler - Ing. Büro Harald Simmler **The Power of High Level Co-Simulation for HDL Designs** (40 min)	Alexander Daum - FH Oberösterreich Studienbetriebs GmbH **RFSoC RoCE Offload - 100Gbit RDMA on FPGAs** (40 min)	

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Thursday, July 3

	Application	Embedded / Vision	AI / ML	Tools & Methodologies	Board Design & Connectivity	Lectorial
9:00 am - 10:30 am	Helmut Demel - Lattice Semiconductor & Wolfgang Loewer - El Camino GmbH **Industrial IoT Challenges and Solutions for Real Time Communication** (40 min)	Ernst Wehlage - plc2 GmbH **Heterogeneous Design Flow with Adaptive SoCs** (40 min)	Thomas Siebert | Altera, an Intel Company **Introduction to Altera® FPGA AI Suite for Altera® FPGAs and Altera's New DSP Block Architecture** (40 min)	Jan Aniol - plc2 Design GmbH **Bridging the Gap: Integrating Software Lifecycles with FPGA Development** (40 min)	Dr. Michael Gude - Cologne Chip AG **GateMate FPGA: Qualification for Radiation-Tolerant Applications** (40 min)	Jens Stapelfeldt & Mario Ruiz - AMD **Agentic AI Design on AMD Ryzen AI (Lecture)** (90 min)
	Stanislaw Klinke - EBV Elektronik GmbH & Co. KG **Leveraging AI Engine in Versal Devices for Optimized DSP Applications** (40 min)	Alexander Flick - plc2 GmbH **System Device Tree: Improved Support for Multicore Systems with AMD Adaptive SoCs** (40 min)	Mustafa Celik - Arrow Electronics & Leo Wiegand - ONE WARE **Ultra-Fast, Customized CNN AI on Any Altera FPGA** (40 min)	Harald Flügel - Arrow Central Europe GmbH **Let Systhesis Do Its Job But Check the Results** (40 min)	Patrick Urban - Cologne Chip AG **GateMate FPGA: High-Speed Transceiver (SerDes) Hands-On** (40 min)	
10:30 - 11:00 am	**Coffee break**					
11:00 am - 12:30 am	Yakup Erdem Yıldız & Fatih Küçük - Bull Technologies **Low Latency Optimized TCP Stack for High Frequency Trading on FPGA** (40 min)	Alexander Wirthmueller - MPSI Technologies GmbH **Implementing and Profiling Collaborative CPU-FPGA Projects with Real-Time Requirements** (40 min)	Armin Faems - Arrow Central Europe GmbH **How to Use the Tensor Mode of the DSP Blocks in ALTERA Agilex 5 FPGAs** (40 min)	Ernst Wehlage - plc2 GmbH **Project-Based and Non-Project-Based Scripting in Vivado** (40 min)	Lukáš Kekely - DynaNIC GmbH **How to Transfer the Shortest Packets at Sustained 400 Gbps over PCIe** (40 min)	Jens Stapelfeldt & Mario Ruiz - AMD **Agentic AI Design on AMD Ryzen AI (Hands-on Tutorial)** (90 min)
	Andreas Schuler & Andreas Braun - Missing Link Electronics GmbH **In-Vehicle Network - Automotive Zonebased Architecture with Time Sensitive Network - AutoTSN** (40 min)	Gordan Galic - Xylon d.o.o. **Versatile Vision AI Framework Lets You Focus on AI Development** (40 min)	Alexander Flick - plc2 GmbH **AI on the Edge: Insights into NN acceleration** (40 min)	Ernst Wehlage - plc2 GmbH **Multi-Run Management Using Vivado** (40 min)	Dr. Harry Commin - Enclustra GmbH **Doubling RFSoC ADC Rate from 5 Gsps to 10 Gsps** (40 min)	
12:30 - 1:30 pm	**Lunch break**					
1:30 pm - 3:00 pm	Angela Gonzalez - PlanV GmbH **Porting and Optimizing CVA6 to Altera FPGAs** (40 min)	Alin-Tudor Sferle - Analog Devices Ulrich Langenbach - Missing Link Electronics **FPGA-Based Highly Configurable and Low-Latency Multi GMSL Camera 10GbE RTP Streaming** (40 min)	Tobias Genzinger - Ingenics Digital GmbH **Hyperparameter Tuning of FPGA-Accelerated Convolutional Neural Network Inference** (40 min)	Ernst Wehlage - plc2 GmbH **Vitis HLS: From Scratch up to New Features** (40 min)	Gianluca Mariani - Lattice Semiconductor **Developing Ethernet Solutions with FPGAs** (40 min)	
	David Kirchner - World of FPGA **How to Drive Parallel High-Speed Circuits from an AMD FPGA** (40 min)	Stanislaw Klinke - EBV Elektronik GmbH & Co. KG **Seamless Integration of Image Processing and ML Acceleration: AMD Ultrascale+ MPSoC and Hailo in Action** (40 min)	Dr. Pedro Machado - Nottingham Trent University **SpikeSteg: Interconnecting Steganography with FPGA Technology Using Spiking Neural Networks** (40 min)	Derek Hagen - AMD **Direct MATLAB® to AMD Vitis HLS Workflow for High-Performance Results** (40 min)	Nicolay Garcia & Tomas Hudson - Monolithic Power Systems GmbH **48V Power Solutions for Modern FPGAs: Featuring Integrated Power Modules** (40 min)	
3:00 - 3:30 pm	**Coffee break**					
3:30 pm - 5:00 pm	Thomas Kuhn - HTV Halbleiter-Test & Vertriebs-GmbH **OSAT – Outsourced Assembly and Test - Services Around the Semiconductor Production in EU** (40 min)	Armin Faems - Arrow Central Europe GmbH **Implementation of MIPI-CSI2 in Altera Agilex 5 FPGAs** (40 min)	Martin Kellermann & Brian Colgan - Microchip Technology GmbH **Bridging the Gap: Get Any Sensor into Nvidia GPUs** (40 min)	Prof. Dirk Koch - Universität Heidelberg **Partial Configuration: Is It Useful or Just an Academic Toy?** (40 min)	Dr. Aurang Zaib - Microchip Technology GmbH **Holistic Approach for Managing Transceiver Designsin Microchip FPGAs** (40 min)	
	Mihaly Nemeth-Csoka - Heitec AG **The Golden Cage of FPGA Vendor Lock-In** (40 min)	Maximilian Werner - Efinix GmbH **MIPI CSI-2/DSI with Efinix FPGA Families** (40 min)	Karl Wachswender - Lattice Semiconductor GmbH **Accelerating Intelligent Edge Systems with Lattice Semiconductor and NVIDIA** (40 min)	Simon Southwell - Wyvern Semiconductors **Wireguard FPGA Advanced Co-Simulation Verification Environment** (40 min)	Michael Freitag - YAGEO Group - KEMET Electronics GmbH **Power Inductor for Point of Load Buck Converter Applications to Support FPGAs** (40 min)	