

DAY 1 | Tuesday, June 30

Welcome Session: Nikolai Krassin PLC2 & Sebastian Gerstl Vogel Communications Group						
OPENING SPEECH: Altera 3.0, Full range Independent FPGA Supplier Thomas Boudrot - Altera						
	Application	Language / Debug / Verification	Architecture	Tools & Methodologies	Safety & Security	Tutorial
8:20 - 8:30 am						
8:30 - 8:55 am						
9:00 am - 10:30 am	<p>Christopher Hatch - AMD AMD Embedded Development Framework – Embedded Software Stacks Supporting Multiple Software Domains Focusing on Open Source for Easier Long-Term Maintenance (40 min)</p>	<p><i>No lecture</i></p>	<p>Dr. Michael Gude - Cologne Chip Time-to-Digital-Converter (TDC) with less than 5ps resolution for GateMate FPGA (40 min)</p>	<p>Stefan Rooseboom - Pro Design Electronic End-of-Production Test Methodology and Automation for FPGA-Based Systems – Lessons Learned from a Concrete Case Study (40 min)</p>	<p>Martin Kellermann - Microchip Technology & Owen Millwood - WIZnet Germany Organic Cybersecurity and Cyberresilience (40 min)</p>	<p>Andy Walton & Pavel Benacek - Pantherun Technologies P4: Flexibility and Quicker Development for FPGA Packet Processing Sub-Systems (90 min)</p>
	<p>David Kirchner - World of FPGA Communication in Multi-FPGA Systems (40 min)</p>	<p>Salma Hamdoun - Arrow Central Europe FPGA Verification and Testing (40 min)</p>	<p>Stefan Unrein - plc2 Design Demystifying the AMD RFSoc (40 min)</p>	<p>Hervé Ratigner - AMD Advancing AMD Vitis™ HLS: Performance-Driven Design and the Path Toward AI-Assisted Development (40 min)</p>	<p>Matti Tommiska - Xiphera Common Framework for FPGA-based Hardware Root of Trust (40 min)</p>	
10:30 - 11:15 am	Coffee Break and Visit of the Exhibition					
11:15 am - 12:45 pm	<p>Maximilian Werner - Efinix Enable Higher System Integration with Efinix's Small Footprint and SiP FPGAs (40 min)</p>	<p>Jim Lewis - SynthWorks Design Tracking Requirements with OSVVM (40 min)</p>	<p>Oner Hanay - INCIRT Redefining the Limits of Data Converters: Power Efficient Fourier-Domain Data Converters for RF-SoC and FPGA Systems (40 min)</p>	<p>Oliver Bründler - Open Logic CDCs, FIFOs, and Width Converters: How to Combine Open Logic Building Blocks Correctly (40 min)</p>	<p>Christian Mueller - Lattice Semiconductor Trusted Resilience Edge: Unified FPGA-TPM for Post-Quantum Cryptography RED & Cyber Resilience Act (40 min)</p>	<p>Ernst Wehlage - PLC2 Design Practice: Clock and Reset Management (90 min)</p>
	<p>Helmut Demel - Lattice Semiconductor SIPHash IP for Embedded Security Enabling RED Compliance and CRA Readiness in Smart ARVR Systems (40 min)</p>	<p>Jim Lewis - SynthWorks Design OSVVM's Advanced Verification Data Structures (40 min)</p>	<p>Fabian Kluge - Efinix Thermal Management on Efinix FPGAs (40 min)</p>	<p>Cagil Gumus - DESY fwk: A Platform-Independent, Open-Source Framework for Heterogeneous SoC Development in Scientific Instrumentation (40 min)</p>	<p>Saadeddine Ben Jemaa - Arrow Central Europe Building Secure FPGA Systems – Protecting IP and Data at the Edge (40 min)</p>	
12:45 - 1:30 pm	Lunch Break and Visit of the Exhibition					
1:30 - 2:10 pm	DIAMOND SPONSOR KEYNOTE SPEECH: Purpose-Built Engines: From Edge Intelligence to Physical AI Michael Hutchison - AMD					
2:10 - 2:15 pm	Change Rooms					
2:15 pm - 3:45 pm	<p>Fabian Kluge - Efinix Highly integrated Low Latency Datapath Designs with Efinix SerDes Devices (40 min)</p>	<p>Espen Tallaksen - EmLogic AS UVVM : The UVM for VHDL – only simpler (40 min)</p>	<p>Bryan Fletcher - AMD Overcoming the Data Explosion: Optimizing Connectivity, Memory, and Compute with AMD Kintex™ UltraScale+™ Gen 2 FPGAs (40 min)</p>	<p>Yılmaz Gürak & Yahya Kaya - Bull Technologies NanoShield: An FPGA-CPU Hybrid Architecture for Ultra-Low Latency Pre-Trade Risk Management in Compliance with MiFID II (40 min)</p>	<p>Ido Wermuth - Arrow Central Europe Introduction to FPGA Security: Building a Hardware Root of Trust (40 min)</p>	<p>∞ In memory of Guy Eschemann ∞</p> <p>Patrick Lehmann - plc2 Design EDA?: Running OSVVM Simulations from Python (90 min)</p>
	<p>Timor Knudsen - AMD Mini-ISP – an Open-Source Image Signal Processor for AMD Adaptive SoCs and FPGAs (40 min)</p>	<p>Espen Tallaksen - EmLogic AS Assertions in VHDL and UVVM, Plus the newest features of UVVM (40 min)</p>	<p>Dr. Jörg Pospiech - ATV Cost-Effective Industrial Functional Nodes with USB 3 on Spartan UltraScale+ Platform (40 min)</p>	<p>Oren Hollander - HandsOn Training Beyond the Bitstream: Protecting Modern FPGAs from Physical Attacks (40 min)</p>	<p>Harald Friedrich - NewTec FPGAs in Safety Critical Applications - Key Considerations, Challenges and Opportunities in Automotive and Industrial Designs (40 min)</p>	
3:45 - 4:30 pm	Coffee Break and Visit of the Exhibition					
4:30 pm - 6:00 pm	<p>Prof. Dr. Bernhard Lang - Hochschule Osnabrück FPGA components for direct AXI-Stream to UDP/IP/Ethernet Networking (40 min)</p>	<p>Matthias Kern - P2L2 Open Source HDL Co-Simulation with AMD Alveo (40 min)</p>	<p>Armin Faems - Arrow Central Europe How to maximize the utilization of GTS Channels in Altera Agilex 3 & 5? (40 min)</p>	<p>Martin Kellermann - Microchip Technology & Martin Jaiser - Pantherun Plug-and-play inline AES-encryptor to protect modern and legacy systems (40 min)</p>	<p>Fabio Caccamo - AMD Designing for Security (40 min)</p>	<p>Dr. Karsten Trott - Xilinx, an AMD Company Performance Improvements of Deep Learning Accelerator Systems (90 min)</p>
	<p>Jonathan Graf - Graf Research Corporation Bitstream Equivalence Checking for High-Assurance FPGA Systems (40 min)</p>	<p>Tommaso De Vivo - XJTAG Making Electronics Under Pressure (40 min)</p>	<p>Afifa Ishtiaq - Altera From Bring-Up to Deployment: High-Speed Transceiver Development on Altera Agilex 5 FPGAs (40 min)</p>	<p>Prof. Dr. Markus Pfaff - FH Oberösterreich Don't! Vol. 2 - Frequently encountered FPGA Design Quirks You better avoid (40 min)</p>	<p>Stephan Strohmeier & Harald Friedrich - NewTec FPGAs, Artificial intelligence and functional safety - is this possible? (40 min)</p>	
from 7:00 pm	The FPGA Conference 2026 - Evening Event @ Motorworld Inn in Munich sponsored by AMD					

DAY 2 Wednesday, July 1						
	Application	Language / Debug / Verification	Architecture	Tools & Methodologies	Embedded / Vision	Tutorial
9:00 am - 10:30 am	Korbinian Wildwasser - Arrow Central Europe & Thomas Siebert - Altera Implementing DDR5 and LPDDR5 EMIF Interfaces on Altera Agilex low-end and mid-range families (40 min)	Tom Richter - The MathWorks From Models to Testbenches: Accelerating FPGA Verification with MATLAB & Simulink (40 min)	Dr. Hardik Shah - Lattice Semiconductor Solving Your Power Puzzle: Lattice FPGAs' Path to Uncompromised Low Power (40 min)	Andreas Büttner - Efinix How-to Run a Efinix FPGA Design Without Leaving the Command Line (40 min)	Wail Alkalbani - Telecommunications Regulatory Authority - Sultanate of Oman RISC-V-Based Cellular Threat Detection (40 min)	Jim Lewis - SynthWorks Design Inc Getting Started with OSVVM, VHDL's #1 Verification Methodology (90 min)
	Alexander Flick - PLC2 Multiboot for Design Variants and Field Update in Adaptive SoCs (40 min)	Martin Heimlicher - Xipera XiperPy from Xipera: Making Hardware Design Accessible to Software Engineers (40 min)	Christian Michel - Lattice Semiconductor Unlock Next-Gen SDR Design for SWaP-C using Lattice FPGAs (40 min)	Ahmad Alothman - Avnet EMG & Martin Kellermann - Microchip Technology Power-Efficiency vs. Performance, Scaling for Power (40 min)	Tolga Sel - Arrow Central Europe MIPI CSI-2 Lab with Agilex3 (40 min)	
10:30 - 11:15 am Coffee Break and Visit of the Exhibition						
11:15 am - 12:45 pm	Thomas Zerrer - Smartlogic PCI Express Data streaming directly into the GPU (40 min)	Adrian Weiland & Patrick Lehmann - plc2 Design Mocking a AMD MPSoC with OSVVM Verification Components (40 min)	Dr. George Athanasiou - CAST Post-Quantum Cyber Resilience for Automotive SoCs: Crypto-Agile FPGA Architectures (40 min)	Marco Höfle - Avnet EMG From C++ to RTL: A practical AMD Vitis™ HLS Example (40 min)	Kevin Keryk - AMD Building Adaptive Systems that Scale, Using Video as an Example Application (40 min)	Tolga Sel - Arrow Central Europe PART2: MIPI CSI-2 Lab with Agilex3 (Hands-on) (90 min)
	Thomas Zerrer - Smartlogic PCI Express Data streaming directly into the GPU (40 min)	Markus Leiter - P2L2 Inside UVVM: Architecture and Design of Custom Verification Components (40 min)	Sheik Abdullah - iWave Global From External RF Chains to Direct RF: A 64GSPS Wideband SDR Architecture (40 min)	Navid Jalali - plc2 Design Visualizing Metrics from AXI Performance Monitors in Prometheus/Grafana (40 min)	Brian Colgan & Martin Kellermann - Microchip Technology FPGA Vision: Bridging and Broadcast (40 min)	
12:45 - 1:30 pm Lunch Break and Visit of the Exhibition						
1:30 - 2:00 pm KEYNOTE SPEECH: Security and Physical AI: FPGA Architectures for Systems That Sense and Act Raemin Wang - Lattice Semiconductor						
2:00 - 2:15 pm Short Break and Change Rooms						
	Application	Language / Debug / Verification	Architecture	Tools & Methodologies	Board Design & Connectivity	Tutorial
2:15 pm - 3:45 pm	Baruch Mitsengendler - The MathWorks Model-Based Deployment of Deep Learning on FPGAs Using a Reusable HDL Processor Architecture (40 min)	Patrick Lehmann & Stefan Unrein - plc2 Design PoC-Library v3.0: AXI4(-Lite) Interconnect Infrastructures (40 min)	Keith Lumsden - AMD AMD Versal™ RF Series: Bridging the Gap Between RF and Digital Compute (40 min)	Oren Hollander - HandsOn Training Don't Just Compile: Outsmarting the Synthesizer for Peak FPGA Performance (40 min)	Alex Lopich - Altera Supercharging HDR Vision: Multi Exposure Fusion and Adaptive Tone Mapping for FPGA Powered Cameras (40 min)	Espen Tallaksen - EmLogic AS The Inside of a Good VHDL Verification Component (90 min)
	Rolf Broeske - SMART Engineering Predictive Thermal Management as the Key to System Reliability (40 min)	Hans-Jürgen Schwender - Var Industries FuSa Compliant Verification Flow with Questa Verification IQ (40 min)	Stefan Unrein - plc2 Design Overcome PCB mistakes with FPGAs (40 min)	Mihaly Nemeth-Csoka - Heitec AG FPGA Development on Linux: The time is now (40 min)	Marco Höfle - Avnet EMG System Simulation of Zynq UltraScale+™ and Versal™ Designs using a MicroBlaze™ V Processor (40 min)	
3:45 - 4:30 pm Coffee Break and Visit of the Exhibition						
4:30 pm - 6:00 pm	Francesco Contu - Avnet EMG Italy Multi-Gigabit Links Optimization and Troubleshooting Using IBERT (40 min)	Michal Pacula - Aldec-Adt Quantum Qiskit HDL Co-Simulation (40 min)	Alexander Flick - PLC2 Versal Adaptive SoC Family: Enhanced Portfolio with Versal AI Edge Gen2 and Versal Prime Series Gen2 (40 min)	Prof. Dr. Bernhard Lang - Hochschule Osnabrück Recycling Tricky Historical Algorithms for FPGA Usage: Toepler's Algorithm for Numerical Root Computation (40 min)	Brian Colgan & Martin Kellermann - Microchip Technology Deterministic Vision and Precision Control Architectures for Humanoid Robots (40 min)	Espen Tallaksen - EmLogic AS Enhanced Randomisation and Functional Coverage, Including the Latest Questa UVVM Extensions (90 min)
	Francesco Contu - Avnet EMG Italy RF_SOC Advanced Usage: Multi-channel and Multi-chip Synchronization (40 min)	Michal Pacula - Aldec-Adt Leveraging 64-bit Integers - Range, Precision, OSVVM AXI and Big Memories for VHDL Designs (40 min)	Karl Wachswender - Lattice Semiconductor Role of Low Power FPGAs in physical AI – Sensor Fusion, Compute Offloading, and Synchronization (40 min)	Dr. Kamil Rudnicki - Brightelligence The Hidden Tax of Bad FPGA Project Methodology (40 min)	Ernst Wehlage - PLC2 AMD FreeRTOS to Zephyr (40 min)	

DAY 3 Thursday, July 2						
	Application	Language / Debug / Verification	Architecture	Tools & Methodologies	Embedded / Vision	Embedded AI Tracks (see next page)
9:00 am - 10:30 am	Dr. Aurang Zaib - Microchip Technology Enabling Low-Latency Applications at the Industrial Edge with FPGA-Based Acceleration (40 min)	Elijah Almeida Coimbra - Topic Embedded Systems Re-use Human-Readable Test Cases for Different Test Levels (Unit/System) Using CocoTB and BDD (40 min)	Ernst Wehlage - PLC2 Understanding the FSBL (40 min)	Prof. Dirk Koch - Universität Heidelberg Open-Source Tools for Commercial FPGAs are There - and There is More to it (40 min)	Alexander Wirthmueller - MPSI Technologies Implementation of a Computer Vision Project on Multiple Platforms (40 min)	
	Alex Lopich - Altera Precision Warping for Advanced Imaging: When Optics Get Weird, FPGAs Step In (40 min)	Peter Fischer - Eccelators Trapped by FPGA Complexity? Applying Software Methodologies to Regain Momentum (40 min)	Timor Knudsen - AMD Overcoming Compute Memory Bottlenecks – It's "On the Package" (40 min)	Oron Port - DFiant Intro to DFHDL, an Opensource Multi-Abstraction Hardware Description Framework (40 min)	Alberto Venzo - Spiral Engineering Image Sensor Integration in FPGA (40 min)	
10:30 - 11:00 am	Coffee Break and Time for Networking					
11:00 am - 12:30 pm	John Heslip - AMD Beyond the Lid: Maximizing Thermal Efficiency in Modern High-Performance Devices (40 min)	Krzysztof Czyz & Mateusz Maciag - Embevity Resource Efficient DMA for FPGA Streaming Pipelines Implemented in SpinalHDL (40 min)	Stefan Garcia - Altera Implementing Real-Time Applications on Modern ARM v8.2-Based FPGA SoCs (40 min)	Alexander Flick - PLC2 Exploring the AMD Adaptive SoC Design Flow with the Vitis(TM) Unified IDE (40 min)	Benjamin Mecke - Arrow Central Europe MIPSI CSI 2 to USB 3.2 Video Pipeline with CrossLinkU NX (40 min)	E m b e d d e d
	Georg Hanak - Achronix Semiconductor Corporation Implementing high-speed FIR Filter in Achronix Speedster7t FPGAs (40 min)	Bernhard Wandl - P2L2 hdl-registers: The Smart Way to Build AXI-Lite IP Cores (40 min)	Angelo Lo Cicero - Altera & Giorgiomaaria Cicero - Accelerat Deterministic Execution of Real-Time Workloads on Agilex 5: a Multi-Domain Approach (40 min)	Ernst Wehlage - PLC2 From PetaLinux to Yocto EDF (40 min)	Atakan Tosun - Heitec Why Not Just Use a GPU? A Critical Case Study of High-Level Synthesis on FPGA vs. CPU and GPU (40 min)	
12:30 - 1:30 pm	Lunch Break and Time for Networking					
1:30 pm - 3:00 pm	Nicolay Garcia - Monolithic Power Systems Space-Optimized PMIC Power Modules for FPGAs: Up to 80% Smaller Total Solution Area (40 min)	Hannes Bachl - Ostbayerische Technische Hochschule Bottom-up Radiation Hardness Assurance for FPGA Based Software Defined Radios (40 min)	Michel Pedimina - Pantherun Pepper: The Open-Source FPGA-Based Rapid Development Board and Environment for Secure Edge Innovation (40 min)	Ernst Wehlage - PLC2 The New Spartan UltraScale+ Family (40 min)	Konstantin Dobrosolets - Altera Technical Advantages of the HyperFlex Gen2 Architecture in Altera Agilex 3 and Agilex 5 FPGAs (40 min)	A I T r a c k s
	Benjamin Mecke - Arrow Central Europe Reset Strategies (40 min)	Patrick Lehmann - plc2 Design EDA?: Post-processing EDA Tool outputs (40 min)	Andreas Schuler - Missing Link Electronics Beyond the Bitstream: Streamlining Heterogeneous Computing with the MLE FPGA Full System Stack (40 min)	Pablo Mendoza Eguiguren - Indra Sistemas A Flexible and Scalable YOLO-Specific DPU for Real-Time FPGA Acceleration (40 min)	Helmut Demel - Lattice Semiconductor Smarter Robotics with Lattice FPGAs: From Vision to Motion (40 min)	
3:00 - 3:30 pm	Coffee Break and Time for Networking					
3:30 pm - 5:00 pm	Matteo Vit - Starware Design PCIe in Embedded FPGA Companion Chips: Implementation, Performance, and Verification (40 min)	Dr. Harald Simmler - Ing. Buero Harald Simmler The Power of High Level Co-Simulation for HDL Designs (40 min)	Armin Faems - Arrow Central Europe Implementation of Nios V with HyperRAM in Altera Agilex FPGA (40 min)	Oliver Bründler - Enclustra Mistakes to Avoid in High-Rate RFSoc Designs (40 min)	Burak Gazel - Aselsan Enabling Fault Tolerance in an FPGA-Based RISC-V Processor Through Lockstep Detection and Replay Recovery (40 min)	
	Christian Michel - Lattice Semiconductor Crypto-Factories: Homomorphic Encryption Powers FPGA-Accelerated Confidential Computing for Industrial Edge AI (40 min)	Denis Vasilik - Eccelators What Software Development Got Right - And FPGA Design Can Now Use (40 min)	Angelo Lo Cicero - Altera Robotics with Altera FPGA (40 min)	Armin Faems & Philipp Henze - Arrow Central Europe Developing with Lattice Propel (40 min)	Volker Urban - Ingenieurbüro Dipl.-Ing. Volker Urban Emulation of Classic CPUs – a SoC-friendly Hybrid Approach (40 min)	

DAY 3 Thursday, July 2				
	Embedded AI - #1	Embedded AI - #2	Embedded AI - #3	Embedded AI - #4
9:00 am - 10:30 am	Alexander Flick - PLC2 AI Basics: From image processing to perception and beyond (40 min)	Yunus Kk & Burak Aykenar - Analogic FPGA-Accelerated Multi-Camera AI Vision for High-Speed Industrial Inspection on Kria KR260 (40 min)	Christian Mueller Lattice Semiconductor Efficient 360° Threat Detection for Parked Vehicles - A Distributed, Event-Driven Approach (40 min)	Alexander Montgomerie-Corcoran - Heronic Technologies Reinventing Super Resolution at the Edge: Custom FPGA AI Engines That Outrun GPUs (40 min)
	Alexander Flick - PLC2 Inside Edge AI: Processing Paradigms and Architectural Hints (40 min)	Karl Wachswender - Lattice Semiconductor Building State of the Art Computer Vision Models for the Far Edge (40 min)	Yashwant Dagar - CraftifAI PipeGen: Agentic AI to Generate, Debug, and Deploy End-to-End Edge AI Pipelines (40 min)	Tolga Sel - Arrow Central Europe & Helmut Pltz - ONE WARE AI for Everyone with Altera Agilex3 (40 min)
10:30 - 11:00 am	Coffee Break and Time for Networking			
11:00 am - 12:30 pm	Saad Qazi - EBV Elektronik Reality Over Peak Specs: Constraints Driven Platform Selection for Edge AI (40 min)	Oren Hollander - HandsOn Training Silicon Brains vs. Silicon Gates: Can LLMs Replace the FPGA Engineer? (40 min)	Dr. Calliope-Louisa Sotiropoulou - CAST Breaking the Data Bottleneck: Hardware-Accelerated Lossless Compression for Next-Generation AI Systems (40 min)	Jimmy Chou - Infineon Technologies Accelerating Adoption of USB 10Gbps I/O in Edge AI and Embedded Systems (90 min)
	Alexander Flick - PLC2 BYOM – Custom Model Edge Inference with Vitis AI (40 min)	Andreas Bttner - Efinix Accelerating Edge AI with Efinix FPGAs: TinyML and eCNN for Real-World Applications (40 min)	Brian Colgan & Martin Kellermann - Microchip Technology One Size Does Not Fit All: Power-Efficient Vision AI on FPGAs and Beyond (40 min)	
12:30 - 1:30 pm	Lunch Break and Time for Networking			
1:30 pm - 3:00 pm	Denis Vasilik - Ecelerators An Experiment in AI-Assisted FSMs on FPGAs (40 min)	Georg Hanak - Achronix Semiconductor Corporation Design Techniques for High-Performance Low-Latency LLM Inferencing on FPGAs optimized for AI (40 min)	Karl Wachswender - Lattice Semiconductor Beyond the "Sledgehammer": Implementing Physical AI at the Sensor to Offload Robotic SoCs (40 min)	Tomasz Iwanski - Arrow Central Europe Altera FPGA AI Suite: A Practical Deep Dive (90 min)
	Dr. Michael Gude - Cologne Chip Next Generation quasi-analog Neuron AI Chip and FPGA (40 min)	David Hintringer - TRS-STAR Low-Power Low-Latency Edge AI with FPGAs: Balancing Performance, Power, and Complexity (40 min)	Gildas Genest - AMD AMD Vitis™ AI Tools Workflow: Compilation, Hardware Deployment & Profiling (40 min)	
3:00 - 3:30 pm	Coffee Break and Time for Networking			
3:30 pm - 5:00 pm	Alexander Flick - PLC2 Beyond the Architecture - A Forensic, Data-Centric Approach to Image Detection (40 min)	Karl Wachswender - Lattice Semiconductor Efficient Vision Pipelines on FPGAs: Design Patterns and Performance Tuning (40 min)	Dr. Aurang Zaib - Microchip Technology Software-to-Hardware Synergy for Edge AI: From Model Compression to Low-Power FPGA Acceleration (40 min)	Luke Millar - AMD Agentic AI in the FPGA Design Loop (90 min)
	Ulrich Schmidt - EBV Elektronik Reimagining Edge GenAI – Generative AI with Hailo-10 (40 min)	Saadeddine Ben Jemaa - Arrow Central Europe Efficient Edge AI Inference on PolarFire SoC FPGAs Using VectorBlox 3.0 Compression Techniques (40 min)	Prof. Hans Dermot Doran - Zurich University of Applied Sciences Dataflow driven Scalable AI Accelerator Architecture for FPGA and eFPGA Platforms (40 min)	