

## DAY 1 | Tuesday, June 30

Welcome Session: Nikolai Krassin   PLC2 & Sebastian Gerstl   Vogel Communications Group						
OPENING SPEECH: Altera 3.0, Full range Independent FPGA Supplier   Thomas Boudrot - Altera						
	Application	Language / Debug / Verification	Architecture	Tools & Methodologies	Safety & Security	Tutorial
8:20 - 8:30 am						
8:30 - 8:55 am						
9:00 am - 10:30 am	<p>Christopher Hatch - AMD <b>AMD Embedded Development Framework – Embedded Software Stacks Supporting Multiple Software Domains Focusing on Open Source for Easier Long-Term Maintenance</b> (40 min)</p>	<p>Salma Hamdoun - Arrow Central Europe <b>FPGA Verification and Testing</b> (40 min)</p>	<p>Dr. Michael Gude - Cologne Chip <b>Time-to-Digital-Converter (TDC) with less than 5ps resolution for GateMate FPGA</b> (40 min)</p>	<p>Stefan Rooseboom - Pro Design Electronic <b>End-of-Production Test Methodology and Automation for FPGA-Based Systems – Lessons Learned from a Concrete Case Study</b> (40 min)</p>	<p>Martin Kellermann - Microchip Technology &amp; Owen Millwood - WIZnet Germany <b>Organic Cybersecurity and Cyberresilience</b> (40 min)</p>	<p>Andy Walton &amp; Pavel Benacek - Pantherun Technologies <b>P4: Flexibility and Quicker Development for FPGA Packet Processing Sub-Systems</b> (90 min)</p>
	<p>David Kirchner - World of FPGA <b>Communication in Multi-FPGA Systems</b> (40 min)</p>	<p>Salma Hamdoun - Arrow Central Europe <b>FPGA Verification and Testing</b> (repetition of the previous lecture) (40 min)</p>	<p>Stefan Unrein - plc2 Design <b>Demystifying the AMD RFSoc</b> (40 min)</p>	<p>Hervé Ratigner - AMD <b>Advancing AMD Vitis™ HLS: Performance-Driven Design and the Path Toward AI-Assisted Development</b> (40 min)</p>	<p>Matti Tommiska - Xiphera <b>Common Framework for FPGA-based Hardware Root of Trust</b> (40 min)</p>	
10:30 - 11:15 am	Coffee Break and Visit of the Exhibition					
11:15 am - 12:45 pm	<p>Maximilian Werner - Efinix <b>Enable Higher System Integration with Efinix's Small Footprint and SIP FPGAs</b> (40 min)</p>	<p>Jim Lewis - SynthWorks Design <b>Tracking Requirements with OSVVM</b> (40 min)</p>	<p>Oner Hanay - INCIRT <b>Redefining the Limits of Data Converters: Power Efficient Fourier-Domain Data Converters for RF-SoC and FPGA Systems</b> (40 min)</p>	<p>Oliver Bründler - Open Logic <b>CDCs, FIFOs, and Width Converters: How to Combine Open Logic Building Blocks Correctly</b> (40 min)</p>	<p>Christian Mueller - Lattice Semiconductor <b>Trusted Resilience Edge: Unified FPGA-TPM for Post-Quantum Cryptography RED &amp; Cyber Resilience Act</b> (40 min)</p>	<p>Ernst Wehlage - PLC2 <b>Design Practice: Clock and Reset Management</b> (90 min)</p>
	<p>Helmut Demel - Lattice Semiconductor <b>SIPHash IP for Embedded Security Enabling RED Compliance and CRA Readiness in Smart ARVR Systems</b> (40 min)</p>	<p>Jim Lewis - SynthWorks Design <b>OSVVM's Advanced Verification Data Structures</b> (40 min)</p>	<p>Fabian Kluge - Efinix <b>Thermal Management on Efinix FPGAs</b> (40 min)</p>	<p>Cagil Gumus - DESY <b>fwk: A Platform-Independent, Open-Source Framework for Heterogeneous SoC Development in Scientific Instrumentation</b> (40 min)</p>	<p>Saadeddine Ben Jemaa - Arrow Central Europe <b>Building Secure FPGA Systems – Protecting IP and Data at the Edge</b> (40 min)</p>	
12:45 - 1:30 pm	Lunch Break and Visit of the Exhibition					
1:30 - 2:10 pm	DIAMOND SPONSOR KEYNOTE SPEECH: Purpose-Built Engines: From Edge Intelligence to Physical AI   Michael Hutchison - AMD					
2:10 - 2:15 pm	Change Rooms					
2:15 pm - 3:45 pm	<p>Fabian Kluge - Efinix <b>Highly integrated Low Latency Datapath Designs with Efinix SerDes Devices</b> (40 min)</p>	<p>Espen Tallaksen - EmLogic AS <b>UVVM : The UVM for VHDL – only simpler</b> (40 min)</p>	<p>Bryan Fletcher - AMD <b>Overcoming the Data Explosion: Optimizing Connectivity, Memory, and Compute with AMD Kintex™ UltraScale+™ Gen 2 FPGAs</b> (40 min)</p>	<p>Yılmaz Gürak &amp; Yahya Kaya - Bull Technologies <b>NanoShield: An FPGA-CPU Hybrid Architecture for Ultra-Low Latency Pre-Trade Risk Management in Compliance with MiFID II</b> (40 min)</p>	<p>Ido Wermuth - Arrow Central Europe <b>Introduction to FPGA Security: Building a Hardware Root of Trust</b> (40 min)</p>	<p style="text-align: center;">∞ In memory of Guy Eschemann ∞</p> <p>Patrick Lehmann - plc2 Design <b>EDA?: Running OSVVM Simulations from Python</b> (90 min)</p>
	<p>Timor Knudsen - AMD <b>Mini-ISP – an Open-Source Image Signal Processor for AMD Adaptive SoCs and FPGAs</b> (40 min)</p>	<p>Espen Tallaksen - EmLogic AS <b>Assertions in VHDL and UVVM, Plus the newest features of UVVM</b> (40 min)</p>	<p>Dr. Jörg Pospiech - ATV <b>Cost-Effective Industrial Functional Nodes with USB 3 on Spartan UltraScale+ Platform</b> (40 min)</p>	<p>Oren Hollander - HandsOn Training <b>Beyond the Bitstream: Protecting Modern FPGAs from Physical Attacks</b> (40 min)</p>	<p>Harald Friedrich - NewTec <b>FPGAs in Safety Critical Applications - Key Considerations, Challenges and Opportunities in Automotive and Industrial Designs</b> (40 min)</p>	
3:45 - 4:30 pm	Coffee Break and Visit of the Exhibition					
4:30 pm - 6:00 pm	<p>Prof. Dr. Bernhard Lang - Hochschule Osnabrück <b>FPGA components for direct AXI-Stream to UDP/IP/Ethernet Networking</b> (40 min)</p>	<p>Matthias Kern - P2L2 <b>Open Source HDL Co-Simulation with AMD Alveo</b> (40 min)</p>	<p>Armin Faems - Arrow Central Europe <b>How to maximize the utilization of GTS Channels in Altera Agilex 3 &amp; 5?</b> (40 min)</p>	<p>Martin Kellermann - Microchip Technology &amp; Martin Jaiser - Pantherun <b>Plug-and-play inline AES-encryptor to protect modern and legacy systems</b> (40 min)</p>	<p>Fabio Caccamo - AMD <b>Designing for Security</b> (40 min)</p>	<p>Dr. Karsten Trott - Xilinx, an AMD Company <b>Performance Improvements of Deep Learning Accelerator Systems</b> (90 min)</p>
	<p>Jonathan Graf - Graf Research Corporation <b>Bitstream Equivalence Checking for High-Assurance FPGA Systems</b> (40 min)</p>	<p>Tommaso De Vivo - XJTAG <b>Making Electronics Under Pressure</b> (40 min)</p>	<p>Afifa Ishtiaq - Altera <b>From Bring-Up to Deployment: High-Speed Transceiver Development on Altera Agilex 5 FPGAs</b> (40 min)</p>	<p>Prof. Dr. Markus Pfaff - FH Oberösterreich <b>Don't! Vol. 2 - Frequently encountered FPGA Design Quirks You better avoid</b> (40 min)</p>	<p>Harald Friedrich &amp; Jeanne Pulvermüller - NewTec <b>FPGAs, Artificial intelligence and functional safety - is this possible?</b> (40 min)</p>	
from 7:00 pm	The FPGA Conference 2026 - Evening Event @ Motorworld Inn in Munich sponsored by AMD					

DAY 2   Wednesday, July 1						
	Application	Language / Debug / Verification	Architecture	Tools & Methodologies	Embedded / Vision	Tutorial
9:00 am - 10:30 am	Korbinian Wildwasser - Arrow Central Europe & Thomas Siebert - Altera <b>Implementing DDR5 and LPDDR5 EMIF Interfaces on Altera Agilex low-end and mid-range families</b> (40 min)	Tom Richter - The MathWorks <b>From Models to Testbenches: Accelerating FPGA Verification with MATLAB &amp; Simulink</b> (40 min)	Dr. Hardik Shah - Lattice Semiconductor <b>Solving Your Power Puzzle: Lattice FPGAs' Path to Uncompromised Low Power</b> (40 min)	Andreas Büttner - Efinix <b>How-to Run a Efinix FPGA Design Without Leaving the Command Line</b> (40 min)	Wail Alkalbani - Telecommunications Regulatory Authority - Sultanate of Oman <b>RISC-V-Based Cellular Threat Detection</b> (40 min)	Jim Lewis - SynthWorks Design Inc <b>Getting Started with OSVVM, VHDL's #1 Verification Methodology</b> (90 min)
	Alexander Flick - PLC2 <b>Multiboot for Design Variants and Field Update in Adaptive SoCs</b> (40 min)	Martin Heimlicher - Xipera <b>XiperPy from Xipera: Making Hardware Design Accessible to Software Engineers</b> (40 min)	Christian Michel - Lattice Semiconductor <b>Unlock Next-Gen SDR Design for SWaP-C using Lattice FPGAs</b> (40 min)	Ahmad Alothman - Avnet EMG & Martin Kellermann - Microchip Technology <b>Power-Efficiency vs. Performance, Scaling for Power</b> (40 min)	Tolga Sel - Arrow Central Europe <b>MIPI CSI-2 Lab with Agilex3</b> (40 min)	
10:30 - 11:15 am Coffee Break and Visit of the Exhibition						
11:15 am - 12:45 pm	Thomas Zerrer - Smartlogic <b>PCI Express Data streaming directly into the GPU</b> (40 min)	Adrian Weiland & Patrick Lehmann - plc2 Design <b>Mocking a AMD MPSoC with OSVVM Verification Components</b> (40 min)	Dr. George Athanasiou - CAST <b>Post-Quantum Cyber Resilience for Automotive SoCs: Crypto-Agile FPGA Architectures</b> (40 min)	Marco Höfle - Avnet EMG <b>From C++ to RTL: A practical AMD Vitis™ HLS Example</b> (40 min)	Kevin Keryk - AMD <b>Building Adaptive Systems that Scale, Using Video as an Example Application</b> (40 min)	Tolga Sel - Arrow Central Europe <b>PART2: MIPI CSI-2 Lab with Agilex3 (Hands-on)</b> (90 min)
	Thomas Zerrer - Smartlogic <b>PCI Express Data streaming directly into the GPU</b> <i>(repetition of the previous lecture)</i> (40 min)	Markus Leiter - P2L2 <b>Inside UVVM: Architecture and Design of Custom Verification Components</b> (40 min)	Sheik Abdullah - iWave Global <b>From External RF Chains to Direct RF: A 64GSPS Wideband SDR Architecture</b> (40 min)	Navid Jalali - plc2 Design <b>Visualizing Metrics from AXI Performance Monitors in Prometheus/Grafana</b> (40 min)	Brian Colgan & Martin Kellermann - Microchip Technology <b>FPGA Vision: Bridging and Broadcast</b> (40 min)	
12:45 - 1:30 pm Lunch Break and Visit of the Exhibition						
1:30 - 2:00 pm <b>KEYNOTE SPEECH: Security and Physical AI: FPGA Architectures for Systems That Sense and Act   Raemin Wang - Lattice Semiconductor</b>						
2:00 - 2:15 pm Short Break and Change Rooms						
	Application	Language / Debug / Verification	Architecture	Tools & Methodologies	Board Design & Connectivity	Tutorial
2:15 pm - 3:45 pm	Baruch Mitsengendler - The MathWorks <b>Model-Based Deployment of Deep Learning on FPGAs Using a Reusable HDL Processor Architecture</b> (40 min)	Patrick Lehmann & Stefan Unrein - plc2 Design <b>PoC-Library v3.0: AXI4(-Lite) Interconnect Infrastructures</b> (40 min)	Keith Lumsden - AMD <b>AMD Versal™ RF Series: Bridging the Gap Between RF and Digital Compute</b> (40 min)	Oren Hollander - HandsOn Training <b>Don't Just Compile: Outsmarting the Synthesizer for Peak FPGA Performance</b> (40 min)	Alex Lopich - Altera <b>Supercharging HDR Vision: Multi Exposure Fusion and Adaptive Tone Mapping for FPGA Powered Cameras</b> (40 min)	Espen Tallaksen - EmLogic AS <b>The Inside of a Good VHDL Verification Component</b> (90 min)
	Rolf Broeske - SMART Engineering <b>Predictive Thermal Management as the Key to System Reliability</b> (40 min)	Hans-Jürgen Schwender - Var Industries <b>FuSa Compliant Verification Flow with Questa Verification IQ</b> (40 min)	Stefan Unrein - plc2 Design <b>Overcome PCB mistakes with FPGAs</b> (40 min)	Mihaly Nemeth-Csoka - Heitec AG <b>FPGA Development on Linux: The time is now</b> (40 min)	Marco Höfle - Avnet EMG <b>System Simulation of Zynq UltraScale+™ and Versal™ Designs using a MicroBlaze™ V Processor</b> (40 min)	
3:45 - 4:30 pm Coffee Break and Visit of the Exhibition						
4:30 pm - 6:00 pm	Francesco Contu - Avnet EMG Italy <b>Multi-Gigabit Links Optimization and Troubleshooting Using IBERT</b> (40 min)	Michal Pacula - Aldec-Adt <b>Quantum Qiskit HDL Co-Simulation</b> (40 min)	Alexander Flick - PLC2 <b>Versal Adaptive SoC Family: Enhanced Portfolio with Versal AI Edge Gen2 and Versal Prime Series Gen2</b> (40 min)	Prof. Dr. Bernhard Lang - Hochschule Osnabrück <b>Recycling Tricky Historical Algorithms for FPGA Usage: Toepler's Algorithm for Numerical Root Computation</b> (40 min)	Brian Colgan & Martin Kellermann - Microchip Technology <b>Deterministic Vision and Precision Control Architectures for Humanoid Robots</b> (40 min)	Espen Tallaksen - EmLogic AS <b>Enhanced Randomisation and Functional Coverage, Including the Latest Questa UVVM Extensions</b> (90 min)
	Francesco Contu - Avnet EMG Italy <b>RF_SOC Advanced Usage: Multi-channel and Multi-chip Synchronization</b> (40 min)	Michal Pacula - Aldec-Adt <b>Leveraging 64-bit Integers - Range, Precision, OSVVM AXI and Big Memories for VHDL Designs</b> (40 min)	Karl Wachswender - Lattice Semiconductor <b>Role of Low Power FPGAs in physical AI – Sensor Fusion, Compute Offloading, and Synchronization</b> (40 min)	Dr. Kamil Rudnicki - Brightelligence <b>The Hidden Tax of Bad FPGA Project Methodology</b> (40 min)	Ernst Wehlage - PLC2 <b>AMD FreeRTOS to Zephyr</b> (40 min)	

DAY 3   Thursday, July 2						
	Application	Language / Debug / Verification	Architecture	Tools & Methodologies	Embedded / Vision	Embedded AI Tracks (see next page)
9:00 am - 10:30 am	Dr. Aurang Zaib - Microchip Technology <b>Enabling Low-Latency Applications at the Industrial Edge with FPGA-Based Acceleration</b> (40 min)	Elijah Almeida Coimbra - Topic Embedded Systems <b>Re-use Human-Readable Test Cases for Different Test Levels (Unit/System) Using CocoTB and BDD</b> (40 min)	Ernst Wehlage - PLC2 <b>Understanding the FSBL</b> (40 min)	Prof. Dirk Koch - Universität Heidelberg <b>Open-Source Tools for Commercial FPGAs are There - and There is More to it</b> (40 min)	Alexander Wirthmueller - MPSI Technologies <b>Implementation of a Computer Vision Project on Multiple Platforms</b> (40 min)	
	Alex Lopich - Altera <b>Precision Warping for Advanced Imaging: When Optics Get Weird, FPGAs Step In</b> (40 min)	Peter Fischer - Ececelators <b>Trapped by FPGA Complexity? Applying Software Methodologies to Regain Momentum</b> (40 min)	Timor Knudsen - AMD <b>Overcoming Compute Memory Bottlenecks – It’s “On the Package”</b> (40 min)	Oron Port - DFiant <b>Intro to DFHDL, an Opensource Multi-Abstraction Hardware Description Framework</b> (40 min)	Alberto Venzo - Spiral Engineering <b>Image Sensor Integration in FPGA</b> (40 min)	
10:30 - 11:00 am	Coffee Break and Time for Networking					
11:00 am - 12:30 pm	John Heslip - AMD <b>Beyond the Lid: Maximizing Thermal Efficiency in Modern High-Performance Devices</b> (40 min)	Krzysztof Czyz & Mateusz Maciag - Embevity <b>Resource Efficient DMA for FPGA Streaming Pipelines Implemented in SpinalHDL</b> (40 min)	Stefan Garcia - Altera <b>Implementing Real-Time Applications on Modern ARM v8.2-Based FPGA SoCs</b> (40 min)	Alexander Flick - PLC2 <b>Exploring the AMD Adaptive SoC Design Flow with the Vitis(TM) Unified IDE</b> (40 min)	Benjamin Mecke - Arrow Central Europe <b>MIPSI CSI 2 to USB 3.2 Video Pipeline with CrossLinkU NX</b> (40 min)	E m b e d d e d
	Georg Hanak - Achronix Semiconductor Corporation <b>Implementing high-speed FIR Filter in Achronix Speedster7t FPGAs</b> (40 min)	Bernhard Wandl - P2L2 <b>hdl-registers: The Smart Way to Build AXI-Lite IP Cores</b> (40 min)	Angelo Lo Cicero - Altera & Giorgiomaaria Cicero - Accelerat <b>Deterministic Execution of Real-Time Workloads on Agilex 5: a Multi-Domain Approach</b> (40 min)	Ernst Wehlage - PLC2 <b>From PetaLinux to Yocto EDF</b> (40 min)	Atakan Tosun - Heitec <b>Why Not Just Use a GPU? A Critical Case Study of High-Level Synthesis on FPGA vs. CPU and GPU</b> (40 min)	
12:30 - 1:30 pm	Lunch Break and Time for Networking					
1:30 pm - 3:00 pm	Nicolay Garcia - Monolithic Power Systems <b>Space-Optimized PMIC Power Modules for FPGAs: Up to 80% Smaller Total Solution Area</b> (40 min)	Hannes Bachl - Ostbayerische Technische Hochschule <b>Bottom-up Radiation Hardness Assurance for FPGA Based Software Defined Radios</b> (40 min)	Michel Pedimina - Pantherun <b>Pepper: The Open-Source FPGA-Based Rapid Development Board and Environment for Secure Edge Innovation</b> (40 min)	Ernst Wehlage - PLC2 <b>The New Spartan UltraScale+ Family</b> (40 min)	Konstantin Dobrosolets - Altera <b>Technical Advantages of the HyperFlex Gen2 Architecture in Altera Agilex 3 and Agilex 5 FPGAs</b> (40 min)	A I T r a c k s
	Benjamin Mecke - Arrow Central Europe <b>Reset Strategies</b> (40 min)	Patrick Lehmann - plc2 Design <b>EDA?: Post-processing EDA Tool outputs</b> (40 min)	Andreas Schuler - Missing Link Electronics <b>Beyond the Bitstream: Streamlining Heterogeneous Computing with the MLE FPGA Full System Stack</b> (40 min)	Pablo Mendoza Eguiguren - Indra Sistemas <b>A Flexible and Scalable YOLO-Specific DPU for Real-Time FPGA Acceleration</b> (40 min)	Helmut Demel - Lattice Semiconductor <b>Smarter Robotics with Lattice FPGAs: From Vision to Motion</b> (40 min)	
3:00 - 3:30 pm	Coffee Break and Time for Networking					
3:30 pm - 5:00 pm	Matteo Vit - Starware Design <b>PCIe in Embedded FPGA Companion Chips: Implementation, Performance, and Verification</b> (40 min)	Dr. Harald Simmler - Ing. Buero Harald Simmler <b>The Power of High Level Co-Simulation for HDL Designs</b> (40 min)	Armin Faems - Arrow Central Europe <b>Implementation of Nios V with HyperRAM in Altera Agilex FPGA</b> (40 min)	Oliver Bründler - Enclustra <b>Mistakes to Avoid in High-Rate RFSoc Designs</b> (40 min)	Burak Gazel - Aselsan <b>Enabling Fault Tolerance in an FPGA-Based RISC-V Processor Through Lockstep Detection and Replay Recovery</b> (40 min)	
	Christian Michel - Lattice Semiconductor <b>Crypto-Factories: Homomorphic Encryption Powers FPGA-Accelerated Confidential Computing for Industrial Edge AI</b> (40 min)	Denis Vasilik - Ececelators <b>What Software Development Got Right - And FPGA Design Can Now Use</b> (40 min)	Angelo Lo Cicero - Altera <b>Robotics with Altera FPGA</b> (40 min)	Armin Faems & Philipp Henze - Arrow Central Europe <b>Developing with Lattice Propel</b> (40 min)	Volker Urban - Ingenieurbüro Dipl.-Ing. Volker Urban <b>Emulation of Classic CPUs – a SoC-friendly Hybrid Approach</b> (40 min)	

DAY 3   Thursday, July 2				
	Embedded AI - #1	Embedded AI - #2	Embedded AI - #3	Embedded AI - #4
9:00 am - 10:30 am	Alexander Flick - PLC2 <b>AI Basics: From image processing to perception and beyond</b> (40 min)	Yunus K�k & Burak Aykenar - Anadologic <b>FPGA-Accelerated Multi-Camera AI Vision for High-Speed Industrial Inspection on Kria KR260</b> (40 min)	Christian Mueller   Lattice Semiconductor <b>Efficient 360° Threat Detection for Parked Vehicles - A Distributed, Event-Driven Approach</b> (40 min)	Alexander Montgomerie-Corcoran - Heronic Technologies <b>Reinventing Super Resolution at the Edge: Custom FPGA AI Engines That Outrun GPUs</b> (40 min)
	Alexander Flick - PLC2 <b>Inside Edge AI: Processing Paradigms and Architectural Hints</b> (40 min)	Karl Wachswender - Lattice Semiconductor <b>Building State of the Art Computer Vision Models for the Far Edge</b> (40 min)	Yashwant Dagar - CraftifAI <b>PipeGen: Agentic AI to Generate, Debug, and Deploy End-to-End Edge AI Pipelines</b> (40 min)	Tolga Sel - Arrow Central Europe & Helmut Pl�tz - ONE WARE <b>AI for Everyone with Altera Agilex3</b> (40 min)
10:30 - 11:00 am	Coffee Break and Time for Networking			
11:00 am - 12:30 pm	Saad Qazi - EBV Elektronik <b>Reality Over Peak Specs: Constraints Driven Platform Selection for Edge AI</b> (40 min)	Oren Hollander - HandsOn Training <b>Silicon Brains vs. Silicon Gates: Can LLMs Replace the FPGA Engineer?</b> (40 min)	Dr. Calliope-Louisa Sotiropoulou - CAST <b>Breaking the Data Bottleneck: Hardware-Accelerated Lossless Compression for Next-Generation AI Systems</b> (40 min)	Jimmy Chou - Infineon Technologies <b>Accelerating Adoption of USB 10Gbps I/O in Edge AI and Embedded Systems</b> (90 min)
	Alexander Flick - PLC2 <b>BYOM – Custom Model Edge Inference with Vitis AI</b> (40 min)	Andreas B�ttner - Efinix <b>Accelerating Edge AI with Efinix FPGAs: TinyML and eCNN for Real-World Applications</b> (40 min)	Brian Colgan & Martin Kellermann - Microchip Technology <b>One Size Does Not Fit All: Power-Efficient Vision AI on FPGAs and Beyond</b> (40 min)	
12:30 - 1:30 pm	Lunch Break and Time for Networking			
1:30 pm - 3:00 pm	Denis Vasilik - Ecelerators <b>An Experiment in AI-Assisted FSMs on FPGAs</b> (40 min)	Georg Hanak - Achronix Semiconductor Corporation <b>Design Techniques for High-Performance Low-Latency LLM Inferencing on FPGAs optimized for AI</b> (40 min)	Karl Wachswender - Lattice Semiconductor <b>Beyond the "Sledgehammer": Implementing Physical AI at the Sensor to Offload Robotic SoCs</b> (40 min)	Tomasz Iwanski - Arrow Central Europe <b>Altera FPGA AI Suite: A Practical Deep Dive</b> (90 min)
	Dr. Michael Gude - Cologne Chip <b>Next Generation quasi-analog Neuron AI Chip and FPGA</b> (40 min)	David Hintringer - TRS-STAR <b>Low-Power Low-Latency Edge AI with FPGAs: Balancing Performance, Power, and Complexity</b> (40 min)	Gildas Genest - AMD <b>AMD Vitis™ AI Tools Workflow: Compilation, Hardware Deployment &amp; Profiling</b> (40 min)	
3:00 - 3:30 pm	Coffee Break and Time for Networking			
3:30 pm - 5:00 pm	Alexander Flick - PLC2 <b>Beyond the Architecture - A Forensic, Data-Centric Approach to Image Detection</b> (40 min)	Karl Wachswender - Lattice Semiconductor <b>Efficient Vision Pipelines on FPGAs: Design Patterns and Performance Tuning</b> (40 min)	Dr. Aurang Zaib - Microchip Technology <b>Software-to-Hardware Synergy for Edge AI: From Model Compression to Low-Power FPGA Acceleration</b> (40 min)	Luke Millar - AMD <b>Agentic AI in the FPGA Design Loop</b> (90 min)
	Ulrich Schmidt - EBV Elektronik <b>Reimagining Edge GenAI – Generative AI with Hailo-10</b> (40 min)	Saadeddine Ben Jemaa - Arrow Central Europe <b>Efficient Edge AI Inference on PolarFire SoC FPGAs Using VectorBlox 3.0 Compression Techniques</b> (40 min)	Prof. Hans Dermot Doran - Zurich University of Applied Sciences <b>Dataflow driven Scalable AI Accelerator Architecture for FPGA and eFPGA Platforms</b> (40 min)	